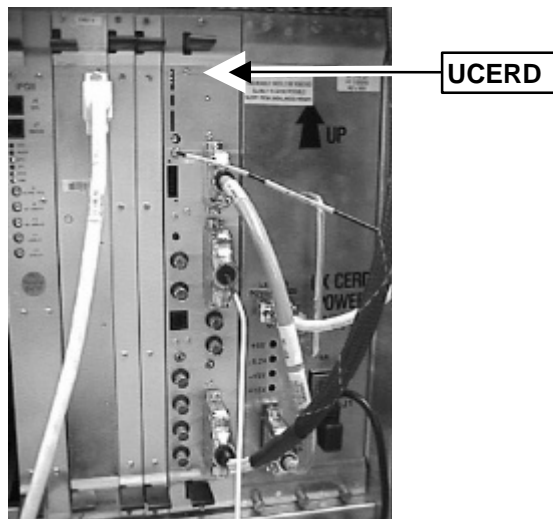


## TABLE OF CONTENTS

TABLE OF CONTENTS .....	1
1 - GENERAL OVERVIEW .....	2
2 - EXCITER THEORY.....	3
3 - RECEIVER THEORY.....	7
4 - DIGITAL BOARD THEORY .....	8
4-1 RAP (Raw Acquisition Processor) .....	10
4-2 CAP (Control Acquisition Processor).....	11
4-3 AIME (Advanced Integer Multiplier Engine).....	12
4-4 ASC (AIME SCHEDULE CONTROLLER).....	12
5 - BUS INTERFACES .....	12
5-1 VME BUS .....	13
5-2 VSB BUS .....	13
5-3 SSP BUS .....	13
5-4 XD BUS .....	13
6 - REPLACEMENT PARTS .....	14
REVISION HISTORY .....	15

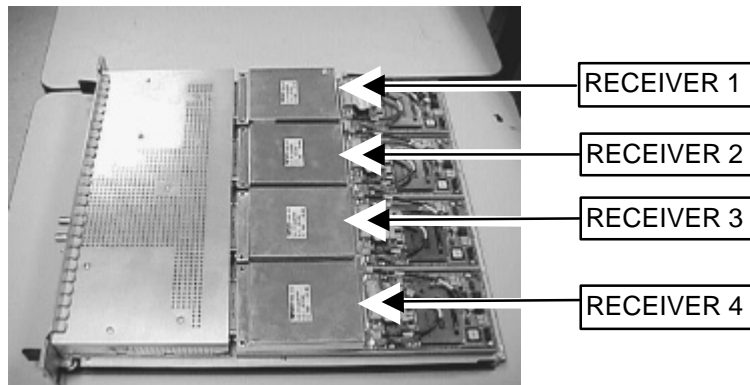
### 1 - GENERAL OVERVIEW

The Universal CERD (UCERD) is a combination of the Exciter, Receiver(s), and Data Acquisition Board (DAB) in one triple-width VME module. The Universal CERD is different from the CERD in that it operates over a frequency range of 8.5 MHz (0.2T) to 170 MHz (4T) without specialized transceiver hardware. It has a consistent output of 4 dBm ( $1.0 V_{pp} \pm 1dBm$ ) ( $0.893 V_{pp}$  to  $1.124V_{pp}$ ) within the frequency range. Although the UCERD has an increased echo bandwidth over the CERD ( $\pm 100kHz$  vs.  $\pm 62.5kHz$ ) it still requires the addition of a Fast Receiver at larger bandwidths for EPI (Echo Planar Imaging). It occupies slots 13, 14, and 15 in the ISE chassis. See illustration 1-1.



**UCERD IN THE ISE CHASSIS**  
ILLUSTRATION 1-1

One-channel and four-channel versions are both available. Systems with the Phased Array option will require a four-channel version. (See Illustration 1-2) Upgrading from one to four channels is accomplished by plugging additional single-channel Receiver boards into the UCERD module. The Digital Board assembly provides the physical support for both the Exciter and the Receivers. It is not necessary to change any jumpers or switches when adding additional Receivers. The additional Receivers will be discovered upon power cycle and download of the TPS.

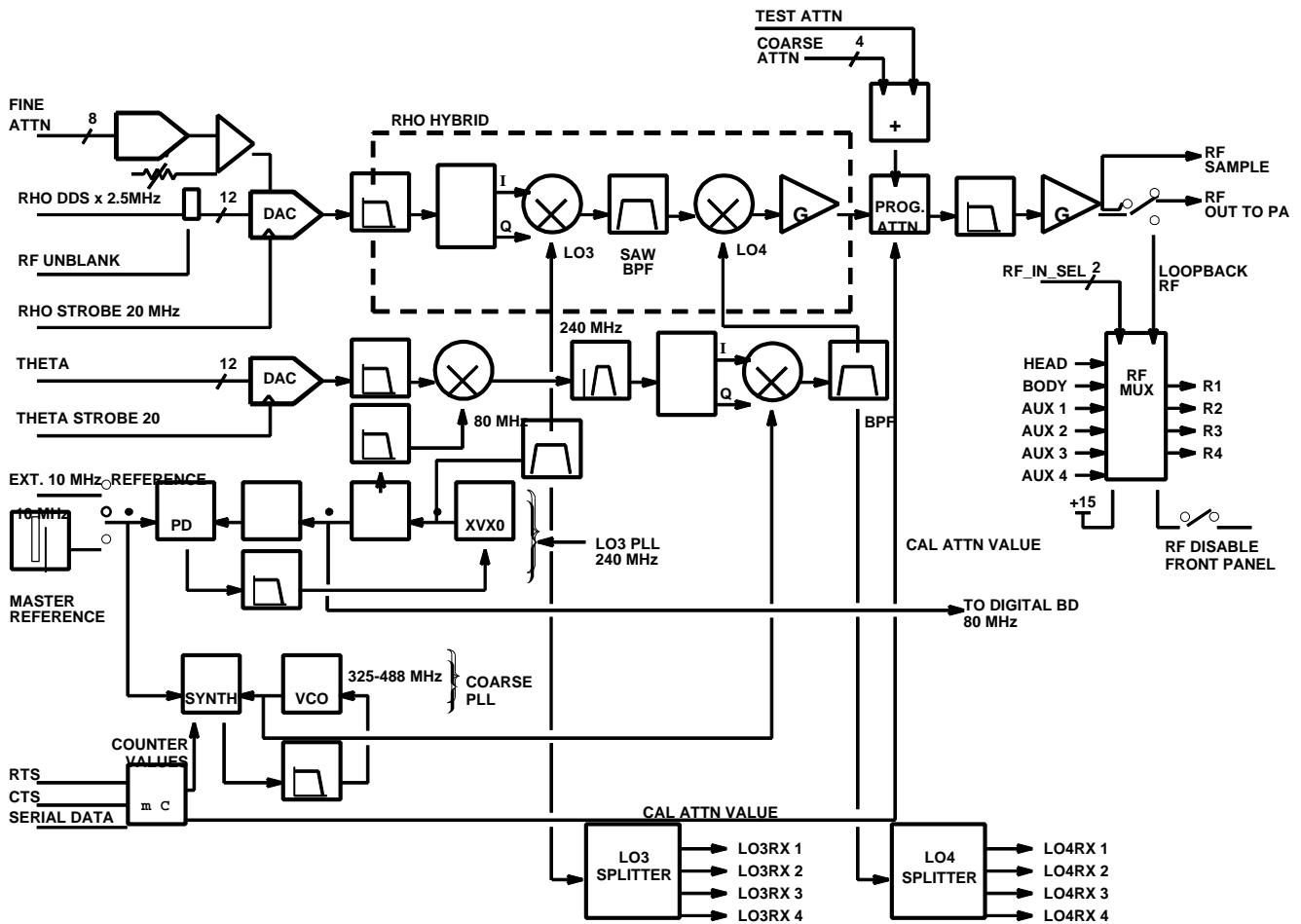


**FOUR CHANNEL UCERD**  
ILLUSTRATION 1-2



The RHO, THETA, and OMEGA signals are passed through a Digital to Analog Converter (DAC) on the Digital Board and a sample can be viewed on J9 on the front of the Digital Board. (Refer to Illustration 2-1)

The UCERD gets its course tuning frequency command (3T, 1.5T, 1.0T) from a microcontroller on the Digital Board. This microcontroller is the interface between the UCERD Digital Board and the Exciter. A single 8 bit value is serially transmitted from the UCERD Digital Board to the Exciter to set the course tuning frequency. The Direct Digital Synthesizer (DDS) provides the fine frequency control to set the final output frequency of the Exciter. The DDS signal is generated at the required frequency (approximately between 3 and 5 MHz) as a 12 bit digital sinewave by the UCERD Digital Board (with RHO, THETA, OMEGA, and FRESBECC inputs from the IPG) and is converted to analog format by a DAC on the Exciter. The Exciter output signal is connected through a directional coupler G2 to provide an accurate test point to view the final output at the front panel. It can be seen on J105 as RF SAMPLE OUT. There is also a switch on the front panel to disable the RF for service. (Refer to Illustration 2-2)



**EXCITER**  
 ILLUSTRATION 2-2

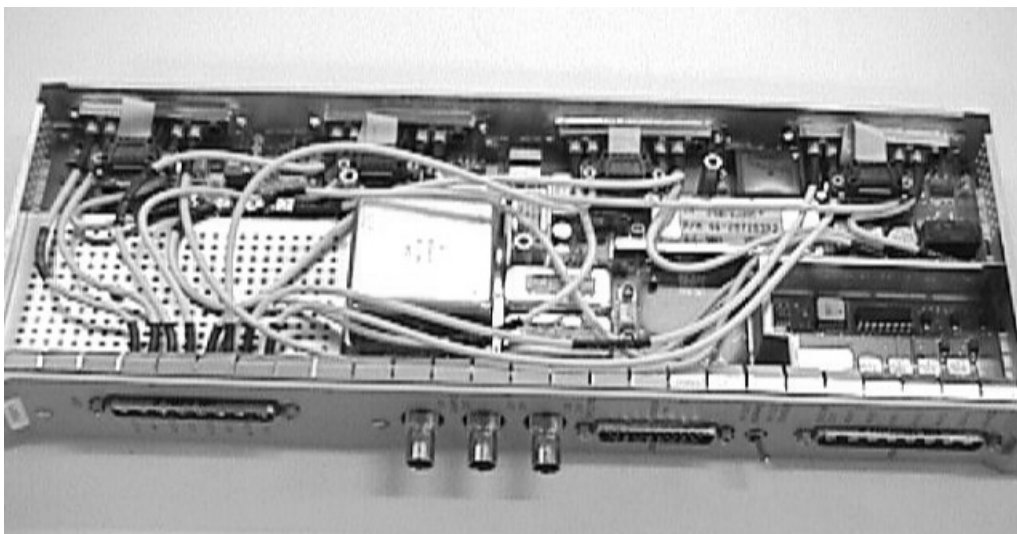
The power for the Receiver preamps can be supplied by the Exciter if there is no TNS connected to the system. A +15VDC supply powers the preamps with a self-resetting polymer fuse device, F1. This device will switch from a low to a high resistance state when a minimum of 2.2 Amps flows through it to the preamps. When in a high resistance state, it will effectively limit the power supply current drawn to about 70 mA. This protects the Exciter circuit traces and preamp coaxial cables in the event of a shorted preamp or cable. The device is self recovering. A voltage comparator circuit is provided to determine when such a fault condition has taken place. The comparator's output will remain low as long as the fuse device is in a low resistance state. While the comparator output is low, a green LED will be illuminated on the front panel.

The Exciter receives power from a 25 pin sub-D connector on the front panel. The corresponding pin-outs are as follows.

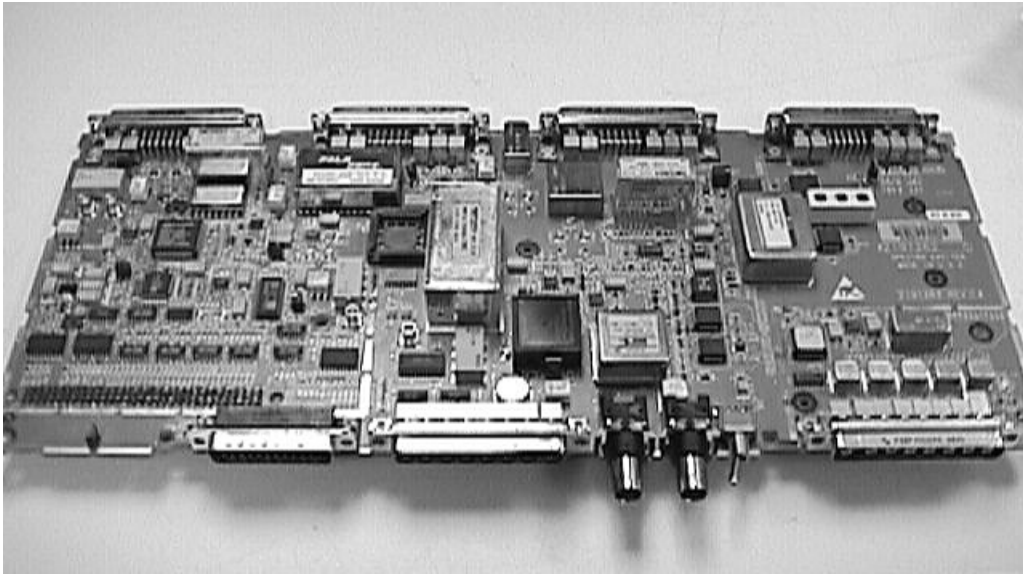
TABLE 2-1  
FRONT PANEL: RF EXCITER BOARD POWER CONNECTOR

Power Supply Voltages	Pin-out* Test Points
+5VDC	1,2,14,15
-5.2VDC	5, 6, 8, 19
+15VDC	9, 10, 11, 12
-15VDC	22, 23
GND:	3,4,7,8,13,16,17,20,21,24,25

Beyond the broadband functionality, the new Exciter also provides service improvements. The previous Exciter utilized discrete coaxial cables to route several of the signals, including the receiver signals. (See Illustration 2-3). This was a serviceability issue, since several of these cables had to be transferred from the Exciter during replacement if the system had multicoil. The cables also produced reliability issues. The new Exciter incorporates transmission line treatment of these signals into the board design. (See Illustration 2-4).



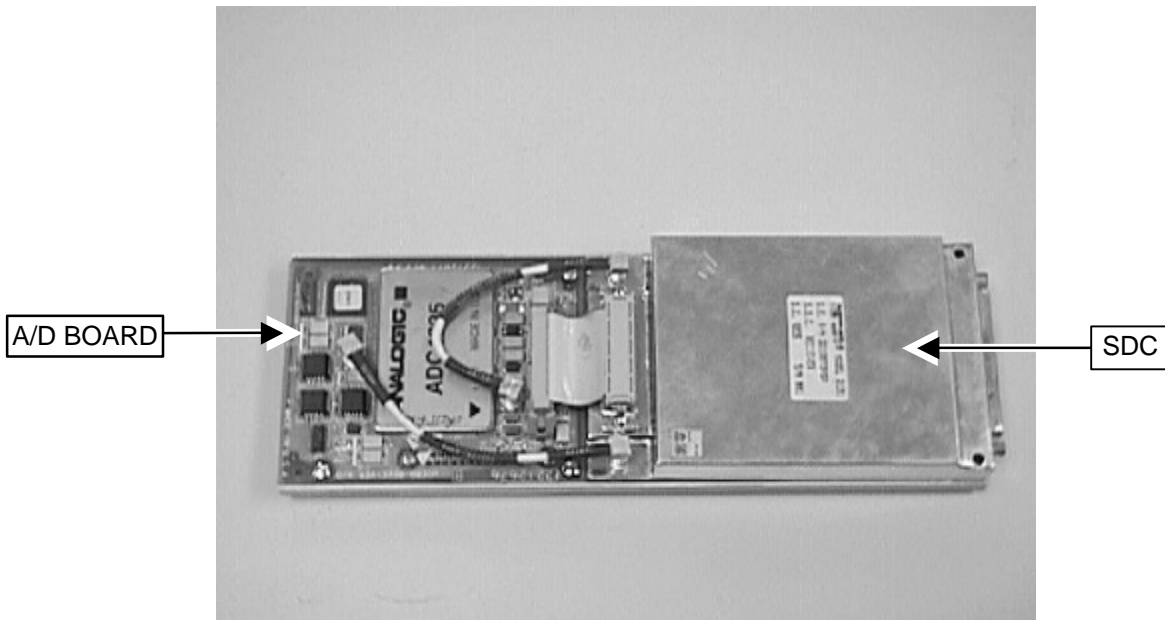
PREVIOUS CERD EXCITER  
ILLUSTRATION 2-3



**NEW UCERD EXCITER**  
ILLUSTRATION 2-4

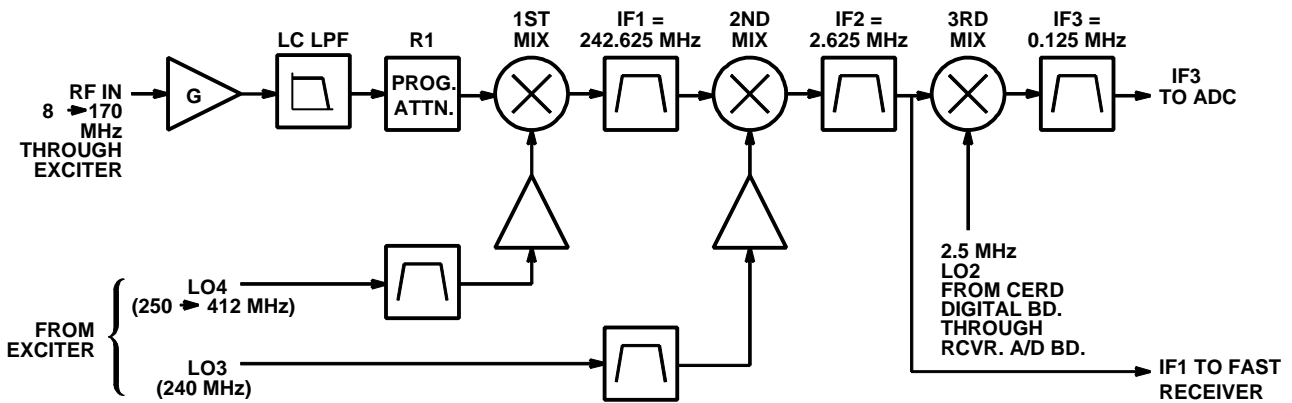
**3 - RECEIVER THEORY**

The Receiver on the UCERD consists of the A/D Board (Analog to Digital) and the SDC (Standard Down Converter). (See Illustration 3-1) The MR signal gets amplified by the receiver preamp, sampled by the TNS (non Spectro receive lines only), input to the Exciter through J109, and then sent to the SDC. The analog signal is then sent to a programmable attenuator (R1) on the SDC. The signal is mixed with a local oscillator resulting in a product at an IF (Intermediate Freq.) of 242.625 MHz. The first IF signal is then applied to a second mixer stage, which combines it with another local oscillator resulting in an IF frequency of 2.625 MHz. At this point, the IF signals are tapped at J101 on the front panel of the UCERD for each Receiver (IF1,IF2,IF3,IF4). IF1 from the first Receiver is used to drive the RF input to the Fast Receiver. The signal is then mixed with another local oscillator from the digital board to produce an IF of 125 KHz. This 125 KHz signal is then sent to the A/D board.(Refer to Illustration 3-2)



**RECEIVER (SDC AND A/D BOARD)**

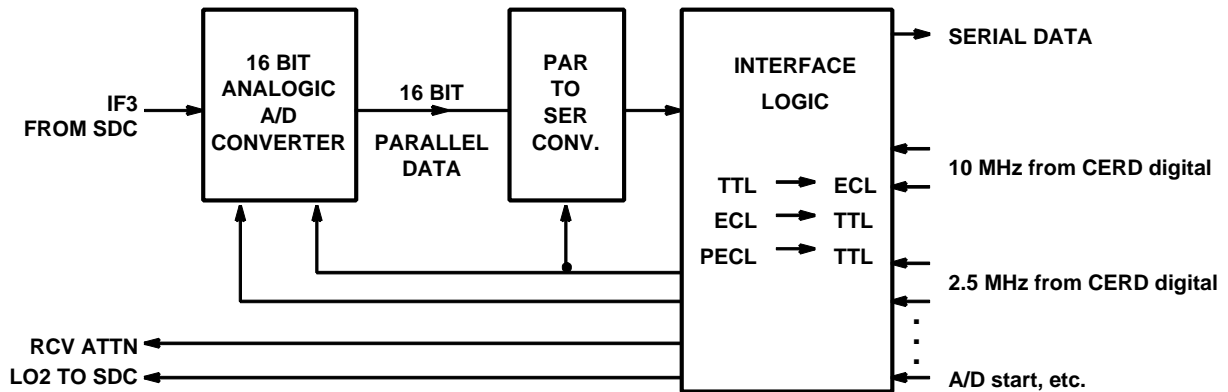
ILLUSTRATION 3-1



**SDC**

ILLUSTRATION 3-2

The Receiver A/D Board interfaces to a 25 pin sub-D connector at each Receiver location on the Digital Board. It interfaces to the SDC through a ribbon cable and two coaxial cables on the front edge of the board. The main function of the A/D Board is to convert the analog signal to digital and convert the digital data from parallel to serial. The signal then gets passed to the Digital Board RAP (Raw Acquisition Processor). (See Illustration 3-3)



**A/D BOARD**  
 ILLUSTRATION 3-3

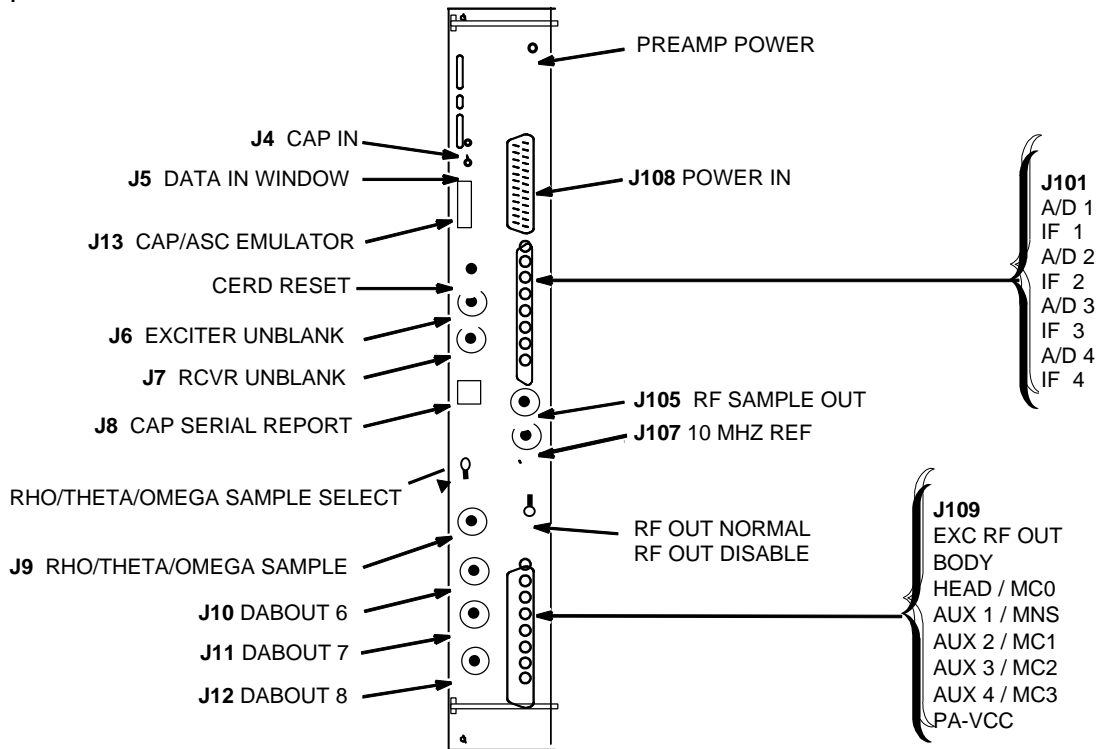
#### 4 - DIGITAL BOARD THEORY

The Digital Board provides the DAB (Data Acquisition Board) function of the UCERD. It is the physical support for the RF Exciter and Receiver modules, and also provides the VME (Versa Module Eurocard) backplane interface for the UCERD. The Digital board consists of the RAP (Raw Acquisition Processor), CAP (Control Acquisition Processor), AIME (Advanced Integer Multiplier Engine), and the ASC (AIME Schedule Controller).

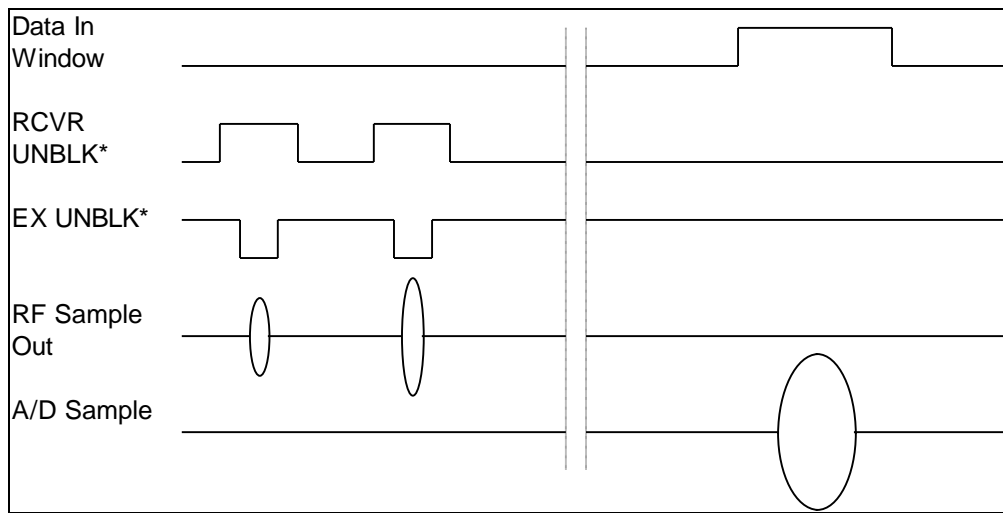
There are several signals that can be monitored on the front panel of the Digital Board. Table 4-1 shows the connectors, while Illustration 4-1 shows the front panel of the UCERD. See Illustration 4-2 for sample waveforms.

TABLE 4-1  
CERD DIGITAL BOARD FRONT PANEL CONNECTORS

Designator		Signal Name	Description	Signal Type
VMX	LX			
J4	same	CAP	Software programmable CAP output	TTL out (1K series resistor)
J5	same	DATA IN WINDOW	RX data in window	TTL out (1K series resistor)
J6	same	EX UNBLK*	RF Exciter Unblank* (was TR Driver Unblank in Signa 5.X)	TTL out (1K series resistor)
J7	same	RCVR UNBLK*	RF RX Unblank*	TTL out (1K series resistor)
J8	same	CAP SERIAL PORT	Serial port out to debug terminal	RS232
J9	same	RHO/THETA/OMEGA SAMPLE	Selectable output to help PSD debug	Analog $\pm 5V$ (1K series resistor)
J10	same	DABOUT 6	(= old DAB J10)	TTL out (1K series resistor)
J11	same	DABOUT 7	(= old DAB J11)	TTL out (1K series resistor)
J12	same	DABOUT 8	(= old DAB J12)	TTL out (1K series resistor)
J13	same	CAP/ASC EMULATOR	TMS320C40 emulator connection	per TMS320C40 User's Guide



UCERD FRONT PANEL  
ILLUSTRATION 4-1



**TYPICAL FRONT PANEL WAVEFORMS**  
ILLUSTRATION 4-2

The Digital Board has 10 LEDs on the front panel. Table 5-2 gives a brief explanation of each LED.

**TABLE 4-2**  
**DIGITAL BOARD LEDs**

LED Name	Color	Description
RXL0	Green	On when LO1 is present on all installed Receivers.
EXL0	Green	On when Exciter 10 Mhz Ref is present and Course Synthesizer is locked
RCVR UNBLK	Green	On when Receiver #1 is unblanked.
EX UNBLK	Green	On when Exciter is unblanked.
CAP	Green	Connected to input line to CAP watchdog. Toggled under software control a minimum of once per second (.5 Hz flash rate minimum).
ASC	Green	Connected to input line to ASC watchdog. Toggled under software control a minimum of once per second (.5 Hz flash rate minimum).
VME	Green	On during VME access to CERD (when slave select signal asserted out of VIC068A). Pulse stretched as required for visibility.
VSB	Green	On during VSB activity. Pulse stretched as required for visibility.
SSP	Green	On during SSP writes to the CERD. Pulse stretched as required for visibility.
XD	Green	On during XD activity. Pulse stretched as required for visibility.

#### 4-1 RAP (Raw Acquisition Processor)

The function of the RAP is to collect data from the receivers, examine the data for overrange, offset correct the data, peak detect the data, test the data against a register-based overrange value, two's complement every other even and odd sample set when quadrature is turned on, queue the data for later use, and write the queued data to QIN memory.

When 1 or 4 CERD receivers are selected, the data from all four are transferred to the RAP (by the RAP) serially at 20 MHz. Because the RAP is generating the conversion and transfer clocks, collecting the CERD receiver data is synchronous.

The RAP performs offset correction to receive data. It does this by adding an offset value, from one of the four offset registers (BL0 through BL3), to the receive data. A value from a particular receiver, along with its offset register, is routed to an adder to obtain the corrected data. All four offset registers are used, along with data from the appropriate receivers during multichannel operation. Offset registers must be loaded with the appropriate values before acquisition begins.

The post offset corrected, peak absolute value from RCVR0 through RCVR3 is furnished via registers PK0 through PK3 respectively for readback by the ASC. The peak absolute value of LXD FIFO data will be on PK0. Because 1) both the data and its two's complement is available in the RAP, 2) implementing peak detection would double the number of peak registers required, and 3) peak detection would have required an additional adder to be implemented, the absolute value is used rather than  $\pm$  peak values.

#### 4-2 CAP (Control Acquisition Processor)

The CAP (formerly known as the DAB) is based on a TMS320C40 digital signal processor running at a clock frequency of 40 MHz. The CAP acts as the central processor of data for the UCERD, and interfaces with most of the UCERD, including the VME bus. The CAP is the UCERD's only interface to the VME bus. The CAP also interfaces with the VSB bus, SSP bus, ASC, AIME, RAP, and Exciter. The CAP controls tasks like where to put the collected data into BAM, the amount of data to be transferred to BAM, and knowing from which Receiver the data is coming from.

The CAP has six communication ports that are used to interface with the other parts of the UCERD.

- COM0 CAP to ASC COM 3
- COM1 CAP to LCA loader
- COM2 CAP to XD Bus LCA
- COM3 ASC COM 0 to CAP
- COM4 SSP PLD to CAP
- COM5 XD Bus LCA to CAP

The ASC (AIME SCHEDULE CONTROLLER) interface to the CAP is very critical as there is a watchdog timer that must communicate with the CAP once every second, or the ASC will be reset. The CAP must monitor the ASC to determine when the ASC has been reset so that the CAP can reload the ASC RAM. Once the ASC has been reset, it will immediately begin monitoring all of its COM ports for activity. The ASC will attempt to boot from any COM port that responds. If the CAP was sending data to the ASC while the ASC was reset, the ASC might misinterpret the stream of data from the CAP as boot data. Because of this possibility, the CAP should force the ASC into reset after the ASC stops communicating with the CAP. Then the CAP can provide the proper data to the ASC for boot loading.

The CAP will boot up from a 128K x 32 FLASH located on the global bus of the C40 processor. The boot FLASH is a block mode type memory with the lowest block of memory fixed and unerasable. All other blocks are erasable and reconfigurable. The intent of the protected boot block is to provide code storage for absolute minimum operation. This includes the code to initialize the C40 processor and set up all the necessary internal functions. It also needs to load the code to test and initialize the VME interface on the CAP. Code also exists to test the rest of the programmable FLASH memory. It could be possible that during a previous programming cycle, power to the board could have been interrupted and the programming did not complete. In this case, the VME chip would be programmed and the UCERD would request that the TARDIS CPU board provide the CERD with new firmware to reprogram the FLASH. In a worst case situation where the protected boot block of the FLASH was working, but the rest of the FLASH could not be reprogrammed, the UCERD should still be able to boot from the TARDIS CPU. This boot process would take much longer, but it would allow the UCERD to function until it could be repaired.

### **4-3 AIME (Advanced Integer Multiplier Engine)**

The AIME exists as a chip set using the Sharp LH9124 digital signal processor (DSP) and the Sharp LH9320 address generator (AG). The LH9124 is a high-performance, fixed-point DSP, optimized for DSP block-oriented algorithms and array processing. Real-time data processing is performed in either the time domain or the frequency domain. The LH9320 AG is a high-speed, memory-addressing device that creates address patterns for the LH9124 data. The AIME is controlled via the AIME Schedule Controller (ASC).

### **4-4 ASC (AIME SCHEDULE CONTROLLER)**

The ASC acts as the control processor for the AIME, and interfaces with most of the CERD modules including the AIME, CAP, and RAP. The ASC has six communication ports which allow it to communicate with the rest of the UCERD. Below is a brief description of the COM ports.

- COM0                      To CAP COM Port 3
- COM1                      To XD Bus LCA
- COM2                      Future
- COM3                      From CAP COM Port 0
- COM4                      Future
- COM5                      Future

The ASC also has a TMS320C40 processor which has a watchdog timer connected to a pin of the C40 processor. If this pin does not change state more often than once every second, the ASC shall be reset. The ASC is also reset during a CAP reset.

## **5 - BUS INTERFACES**

The UCERD interfaces with the rest of the TPS using several different busses. There are four major busses which the UCERD uses. All of these busses are connected to the CAP.

- VME BUS

- VSB BUS
- SSP BUS
- XD BUS

### 5-1 VME BUS

The VME (Versa Module Eurocard) bus interface is located on the UCERD Digital Board. It is configured as a VME Slave device mapped into both short and standard address space. The Cypress VIC068A (VIC) is used as the VME interface. The VME bus interfaces with three areas of the UCERD, including the VME dual port RAM, the test bus controller, and the UCERD board reset register. There is an LED on the front panel to indicate UCERD VME access.

The UCERD interfaces to the VME Backplane through two 3-row (96-pin) and one 5-row (160-pin) DIN connectors. The primary signals on each connector are listed below.

- J1: 3-row - VMEbus
- J2: 5-row - VMEbus on Row b, VSB on Rows a & c, RHO bus on Row d, and THETA Bus on Row e
- J3: 3-row - SSP Bus, XD Bus, DABOUT's, XVRCLK (20MHz), RF unblank's, and B0 compensation

### 5-2 VSB BUS

The UCERD VSB is an arbitrated master-only interface. Only those features required for high performance data transfers are supported by it. This includes transferring data to and from BAM. The VSB bus is a 32-bit multiplexed address/data bus. The CAP interfaces with the VSB bus through a bi-directional dual-port RAM (DPR). The RAM has two logical banks to allow the CAP to continue data transfers while the VSB bus is active. A DMA controller is implemented in the hardware to transfer data between the UCERD and BAM over the VSB bus. The CAP interfaces with the VSB DMA controller over a 16-bit data bus. Upon completion of the transfer(s), the VSB DMA controller asserts an interrupt to the CAP. If, for some reason, no VSB slave responds to the VSB DMA controller within 1.6  $\mu$ s, an interrupt is generated to the CAP, indicating a transfer error. The transfer is terminated.

### 5-3 SSP BUS

The UCERD SSP Bus is a receive only bus. The UCERD cannot write to the SSP Bus. The SSP Bus interfaces with the CAP processor (C40) on COM4. The IPG drives the SSP Bus for diagnostics.

### 5-4 XD BUS

The XD Bus is used for external devices, such as the Fast Receiver in EPI. The CAP interfaces with the XD Bus controller using COM 2 to send data, and COM5 to receive data. The CAP routes the data from XD Bus to the RAP for filtering by the AIME.

## **6 - REPLACEMENT PARTS**

The following parts are FRU's for the UCERD and replacements are available through GPO.

UCERD Assembly - 2221400

UCERD Digital Board - 2206099

Multifreq Receiver Board - 2206100

Multifreq Exciter Board - 2221399

## REVISION HISTORY

REV	DATE	AUTHOR	PRIMARY REASONS FOR CHANGE
A	Oct 26, 1998	R. Kaufman	Preliminary Release for MNS
0	Dec 9, 1998	R. Kaufman	Drawing updates, configup, miscellaneous other changes
1	Dec 16, 1998	R. Kaufman	Misc. Updates.
2	Aug. 16, 1999	R. Kaufman	Converted to ENCORE UCERD Theory. Deleted MNS info.
3	Oct 13, 1999	M. Keber	Added correct proprietary heading to document.