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1- OVERVIEW

The frequency of operation is 29.8MHz +/-500kHz.

The 0.7T RFI (RF Interface Module) consists of four assemblies; the Interface Translator Module, the Input Conditioning Module, the Output Module, and the top level assembly. The top level assembly consists of a chassis, a three-phase circuit breaker (uses only single phase), an “RFI POWER” toggle switch and line fuses. The RFI POWER is a commercially available power supply that supplies DC power to the RFI circuits and power cables. This brings the single -phase line to the circuit breaker and supplies single phase 208V power from the circuit breaker to the RF Amplifier. The RFI functions as an interface between the SSM (System Support Module) and the RF Amplifier with each module performing functions associated with its title.

2- INTERFACE TRANSLATOR MODULE AND FIRMWARE

The Interface Translator is the communication link between the SSM and the RF Amplifier. The GENERAL COMM interface between the SSM and the RFI includes RS-232, UNBLANK, and power monitor fault signals. The power monitor fault signals, MON1, MON2, and HVRLY, are generated by the SSM. The SSM is also the source of UNBLANK.

The interface to the RF Power Amplifier (AMP 1 COMM) contains amplifier control signals such as MAINPWR1 (amplifier enable signal), RESET (for resetting faults), and UNBLANK as well as 6 bits of read-only amplifier status information (STATUS 0 - STATUS 5). MAINPWR1 and UNBLANK signals are outputs of the ISPLSI2032 EPLD. The RESET signal originates in the MC68HC811E2FN microprocessor. Amplifier status information (STATUS 0 - STATUS 5) is read by the microprocessor and made available to the GENERAL COMM interface via RS-232 for error reporting. Amplifier status bits (STATUS 0, STATUS 1, STATUS 5) are also used by the EPLD as a condition for unblanking the amplifier and asserting the MAINPWR1 enable signal.

The Translator can be functionally divided into two sections: the interface with the RS-232 port and the interface with the amplifier port. There is only a small overlap between these two functions. The MC68HC811E2FN (and the associated firmware) handles all of the RS-232 interface functions and a portion of the amplifier interface while the ISPLSI2032 (EPLD) handles only amplifier related functions. The interface between the microprocessor and the EPLD is a small number of digital signals that appear in Table 2-1 below. Also listed in Table 2-1 are signals from the microprocessor which directly control the RF Amplifier via the AMP 1 COMM port.

2- INTERFACE TRANSLATOR MODULE AND FIRMWARE (continued)

TABLE 2-1
CONTROL SIGNALS FROM MICROPROCESSOR

Signal Name	Signal Direction	Description
RESET	from micro to output buffer (AMP 1 COMM)	Set whenever the RFI is in the “off” state. Cleared otherwise
/MAINPWR2 (AC1)	from micro to output buffer (AMP 1 COMM)	always the opposite of OPERATE command.
OPERATE	from micro to EPLD	Set whenever the RFI is in the “operate” state; cleared while in “off” or “standby”
BODYMODE	from micro to EPLD	Set in Body or Test modes, cleared in Head mode.
TESTMODE	from micro to EPLD	Set in Test mode, cleared in Head or Body mode.
NOT-LOCAL-FAULT	from micro to EPLD	Set whenever the micro ‘sees’ no faults.

The EPLD controls the RF Amplifier via the MAINPWR1 and UNBLANK signals. As shown in Table 2-2 below, the value of these signals is dependent on signals from the microprocessor and signals (MON1, MON2, and HVRLY) from the GENERAL COMM port.

TABLE 2-2
Control Signals from EPLD

Signal Name	Signal Direction	Description
/MAINPWR1 (AC2)	from EPLD to output buffer (AMP 1 COMM)	low if OPERATE signal (from micro) is high and no power monitor faults have been detected on the GENERAL COMM port (MON1=0, MON2=0, HVRLY=0).
/UNBLANK	from EPLD to output buffer (AMP 1 COMM)	unblanking occurs if /MAINPWR1 is low, the RF amplifier is not reporting any faults (AMP1 S5=0), the RF amplifier is in operate mode (AMP1 S0=1, AMP1 S1=0), and NOT-LOCAL-FAULT=1

2-1 RS-232 Functions

The microprocessor, U9, responds to all of the RS-232 commands from the SSM and asserts the appropriate digital signals. In addition, the microprocessor enables a periodic timer interrupt (running at 1.00kHz) for the purpose of assessing most of the fault conditions. The functions specifically handled by the microprocessor, divided into 2 categories, are:

Memory Writes:

MW3001 00	Results in setting the “off” bit (Port B bit 3) and clearing the “operate” bit (Port B bit 7).
MW3001 01	Results in clearing both the “off” bit.
MW3001 03	Results in clearing the “off” bit and setting the “operate” bit.
MW3002 20	Invokes the “test mode” bit.
MW3002 40	Invokes the “head mode” bit.
MW3002 60	Invokes the “body mode” bit.
MW3003 50	Default frequency code value, read only register.
Not Local fault:	Updated by the processor asynchronously by the main timer ‘tick’ interrupt routine every 1.00ms. This bit (Port B bit 1) is cleared whenever the processor is aware of the presence of any fault (other than “mode fault”). It is set otherwise. All of the fault conditions which are tested by this interrupt condition are described below. Note: There is only one fault condition (the mode fault) which is not sampled by the main timer interrupt.

Memory Reads:

MR3011	Results in reading the “status byte” which is fully defined in the 0.7T RF Interface Purchase Specification (2244580psp) section 3.2.
MR3012	Results in reading the mode of operation.
MR3013	Results in reading the value of the frequency code.
MR3014	Results in reading and transferring the “fault” byte. A complete list of the fault codes decoded by the translator appears in Table 2-3 below.

2-1 RS-232 Functions (continued)

TABLE 2-3
FAULT CODES

The RFI, in addition to reporting error/status presented on the amplifier interface connections, will also report and indicate internally generated faults.

ERROR /STATUS	CONDITION	RESULTS
HVRLY low	Power Monitor Fault	Set PMON LED. Communicate error code Hex 32
General Overheat Fault	RFI has exceeded maximum temperature	Set Fault LED. Communicate error code Hex 20.
Head Mode	na	Switch to Head mode SET HEAD LED
Body Mode	na	Switch to Body Mode SET BODY LED
Amplifier cable fault	Bad or disconnected cable between RFI and Amplifier	Set FAULT LED. Communicate error code Hex 22
Power Monitor 1 Fault	Safety limit allowed for scan parameters has been reached.	Set PMON LED. Communicate error code Hex 30
Power Monitor 2 Fault	Safety limit allowed for scan parameters has been reached.	Set PMON LED. Communicate error code Hex 31

2-2 Digital Status Signal Bit Definition from RFI

TABLE 2-4
STATUS DEFINITION

STATUS BIT msb lsb	STATUS CODE from RF Amp	Translation AMP	DEFINITION
000000	Hex 00	na	No Power to RF Amplifier. RF Amplifier Interface not active. Power off mode.
000001	Hex 01	na	Operate Mode. Ready for RF.
000010	Hex 02	na	Transient State (Preparing for operation). Follows Main_Power1&2
000011	Hex 03	na	Low Power Dissipation- System Idle.
000100 ≡ 011111	Hex 04 ≡ Hex 1F	na	Not Used.
100000	Hex 20	40	RF Amplifier Power Loss Condition.
100001	Hex 21	41	Power Supply Fault.
100010	Hex 22	42	Duty cycle fault. Unblank duty cycle exceeds specification.
100011	Hex 23	43	I Peak Ovld.
100100	Hex 24	44	Device Fault. RF FET device is shorted.
100101	Hex 25	45	HV Low: Power supply voltage low.
100110	Hex 26	46	HV High: Power supply voltage high.
100111	Hex 27	47	Not Used.
101000	Hex 28	48	Drive level exceeds specification.
101001	Hex 29	49	HEAT. RF Heat sink temperature exceeds 80deg C.
101010	Hex 2A	4A	PEAK POWER. Peak Power from amplifier exceeds specification.
101011	Hex 2B	4B	AVGPWR. Average power from amplifier exceeds specification
101100	Hex 2C	4C	VSWR. Load VSWR exceeds specification.
101101	Hex 2D	4D	GATE. Unblank gate length exceeds specification.
101110	Hex 2E	4E	Junction Temp Fault. RF device junction temperature.
101111	Hex 2F	4F	Undefined fault.

General Debugging Notes

1. The board operates off a single 5VDC supply at about 200mA. The RS-232 line voltages are generated by switchers in the Max232A chip.

Note

The Max232A uses 0.1μF caps in the switchers while the Max232 uses 1.0μF caps.

3- INPUT CONDITIONING MODULE

The Input Conditioning Module is the low-power RF section of the RF Interface. Its purpose is to perform the primary functions listed below:

- Head/Body Drive Level Setting.
- Blanking and Mode Selection.
- Drive and Test Signal Amplification.

In addition to the primary functions listed above, the Input Conditioning Module also serves as an interface between the Translator Module and all other RFI circuitry. This interface includes four digital control signals: HEAD, BODY, TEST, and UNBLANK. Test points are installed on the Input Conditioning Board for each of these four control signals. The +5VDC supply for the CPU is routed through the Input Conditioning Board to the Translator Module, J25-10.

3-1 Head/Body Drive Level Setting

The RF INPUT (J14) is AC coupled by capacitor C1. Head and body drive levels are set by way of two variable resistive attenuators. R2 and the potentiometer R7 form a voltage divider that is used to set the body drive level. This divider is adjustable between 0dB and 16dB of attenuation so that the 10dB range of input power levels is easily accommodated. The body mode drive signal passes from the wiper of potentiometer R7 to pin #5 of the analog multiplexer (U1). D1 and D2 protect the module from overvoltage conditions on the input. The head mode drive signal (pin #4 of U1) is taken from the wiper of potentiometer R12 which, together with R11 and R13, forms a divider and attenuates the body mode drive signal by an additional 7dB to 13dB. As a result of this arrangement, the head drive level is directly affected by the body drive level adjustment. Therefore, the body drive level must always be set before the head drive level.

3-2 Blanking and Mode Selection

The HEAD, BODY, and TEST signals are all active high and only one is high at any point in time. The status of these signals determines which mode the RFI is operating in. The mode of operation is indicated by the HEAD and BODY LEDs on the Translator Board which mount on the front panel of the RFI unit. If both LEDs are off, the RFI is in test mode.

Drive signal blanking is accomplished by the analog multiplexer (U1) which is also used to select between the head and body drive levels. In order to achieve better than 40dB of blanking, a 74HC4052 dual analog multiplexer is used with the output of the first switch fed back to the inputs of the second switch. The multiplexers in the 74HC4052 are 1 of 4 switches. Only two of the inputs to each switch are used. All unused inputs are grounded.

The channel select inputs of the 74HC4052 are driven by the UNBLANK and HEAD control signals which pass from the Translator Board to the Input Conditioning Board on pins J25-9 and J25-6, respectively. When the HEAD signal is high AND the UNBLANK signal is high, the head mode drive signal (on pin #4 of U1) is connected to the output of U1 (pin #13). When the HEAD signal is low AND the UNBLANK signal is high, the body mode drive signal (on pin #5 of U1) is connected to the output of U1 (pin #13). For all other conditions the output of U1 is connected to the unused (grounded) inputs. L1 compensates for the inherent shunt capacitance of U1. This compensation improves input SWR.

The TEST control signal passes from the Translator Board to the Input Conditioning Board on pin J25-7. For test mode, the TEST signal is high. Q1 turns on and pulls the gate of Q2 low. Q2 turns on and supplies 15V to the supply pin of the MHW591 (U3) thus allowing the pulsed drive signal to be amplified and emerge at the RF TEST PORT (J13).

3-3 Head/Body Relay Drivers

The BODY control signal passes from the Translator Board to the Input Conditioning Board on pin J25-5. This signal and the HEAD signal are used to drive the head and body relay drivers. When the HEAD signal is high, Q4 turns on and pulls down the base of Q3 which turns on Q3. The coil of the head relay is connected from the collector of Q3 to the -15V supply. Therefore, when Q3 is turned on, the voltage across the coil is approximately 20V and the head relay is energized. The body relay driver functions in an identical way.

3-4 Drive and Test Signal Amplification

From the output of U1, the drive signal goes to the input of a CLC449 op-amp gain stage (U4). This stage amplifies the drive signal by approximately 12dB.

The input drive to the MHW591 (U3) is taken from the wiper of potentiometer R4 which, together with R6 and R16, forms a divider to attenuate the drive signal by 9dB to 18dB. This allows the output of the test amplifier to be set at precisely 400mW (26dBm) with a nominal 0dBm signal at the RF INPUT (J14).

Note

In TEST mode the amplifier drive output is active at the body power level, but the amplifier is not unblanked.

3-5 Amplifier Drive Level and Phase Balancing

The PHASE BALANCE and GAIN BALANCE adjustments are not applicable because the 0.7T system has a single RF Amplifier Module.

The output signal from J11, AMP1Drive, to the RF Amplifier passes through a CLC449 differential amplifier (U7). A 47.5Ω resistor (R28) is placed in series with the output of the amplifier to create a 50Ω (50 ohm) source impedance. The AMP 1 DRIVE (J11) output is AC coupled through C24.

4- OUTPUT MODULE

The Output Module is the high-power section of the RF Interface. Its purpose is to perform the four primary functions listed below:

- Head / Body Switching.
- Patient Safety Power Monitoring.
- PIN Switch Bias Filtering.

The frequency of operation is 29.8MHz +/-500kHz.

4-1 In-Phase Power Combining

The output of RF Power Amplifier does not require combining.

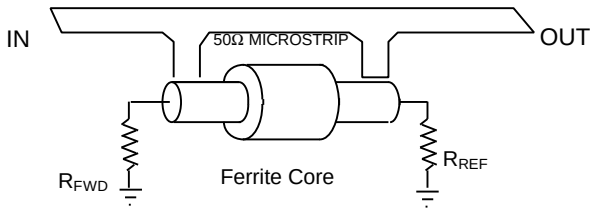
4-2 Head/Body Switching

Switching between head and body mode is accomplished by way of two vacuum relays. The relay driver circuitry is located on the Input Conditioning Board. The output of the power combiner is connected to the normally open pin of both relays. The normally closed pin of each relay is grounded. For head mode, the head relay is energized and the body relay is off. Contact is made between the output of the power combiner and the common pin (pole) of the head relay. For body mode, the body relay is energized and the head relay is off. Contact is made between the output of the power combiner and the common pin (pole) of the body relay. In each case, the common pin (pole) of the off relay is grounded. This arrangement provides better head/body isolation than would be possible with a single relay of this type.

4-3 Patient Safety Power Monitoring

Forward power monitoring is accomplished by way of two pairs of directional couplers (a pair for the head mode signal path and a pair for the body mode signal path). Each pair of directional couplers provides two independent forward power samples for redundant patient safety monitoring. The head directional couplers, DC1 & 2, have a coupling coefficient of -35dB. The body directional couplers, DC 3 &4, have a coupling coefficient of -46dB.

The head and body couplers both work on the same basic principals. The shield of a length of coax is connected in parallel with a length of the primary transmission line (in this case a 50Ω microstrip). During operation, a voltage will exist across the length of the transmission line (and hence across the length of the shield) due to current flow and phase delay. A ferrite core suppresses common mode currents in the coax causing the coax to function like a transformer.



CURRENT FLOW
ILLUSTRATION 4-1

The voltage across the length of the shield causes a small current to flow along the shield which in turn causes a magnetically coupled current to flow through the center conductor. This current flows from the reverse termination (R_{REF}) to the forward termination (R_{FWD}) and results in voltages of opposite polarities at the terminations. Voltage is electrically coupled through the distributed capacitance of the coax with the same polarity at the forward and reverse terminations. In the case of zero reflected power, the voltages due to magnetic and capacitive coupling add at the forward port and cancel at the reflected port. The forward termination consists of a variable resistive attenuator pad which is adjusted in production to obtain precisely the correct coupling coefficient.

4-4 PIN Switch Bias Filtering

During transmission, a positive DC bias is applied to the output in order to forward bias a PIN diode T/R switch. While receiving, a negative DC voltage is applied to the output in order to reverse bias the PIN diode T/R switch. In head mode, the DC bias current is fed through the HEAD TR port (J9) and passes through L4 and L2 on its way to the HEAD OUTPUT (J3). The DC is blocked by capacitors C3 and C11. C6 and C7 interact with L2 and L4 to provide enough filtering to prevent the PIN switch driver from being corrupted by RF. In body mode, the DC bias current is fed through the BODY TR port (J10) and passes through L5 and L3 on its way to the BODY OUTPUT (J4). The DC is blocked by capacitors C4 and C5. C8 and C9 interact with L3 and L5 to provide enough filtering to prevent the PIN switch driver from being corrupted by RF.

REVISION HISTORY

REV	DATE	AUTHOR	PRIMARY REASONS FOR CHANGE
A	August 12, 1999	Resa Lambert	Preliminary Release
0	January 10, 2000	Resa Lambert	Initial Release