TABLE OF CONTENTS

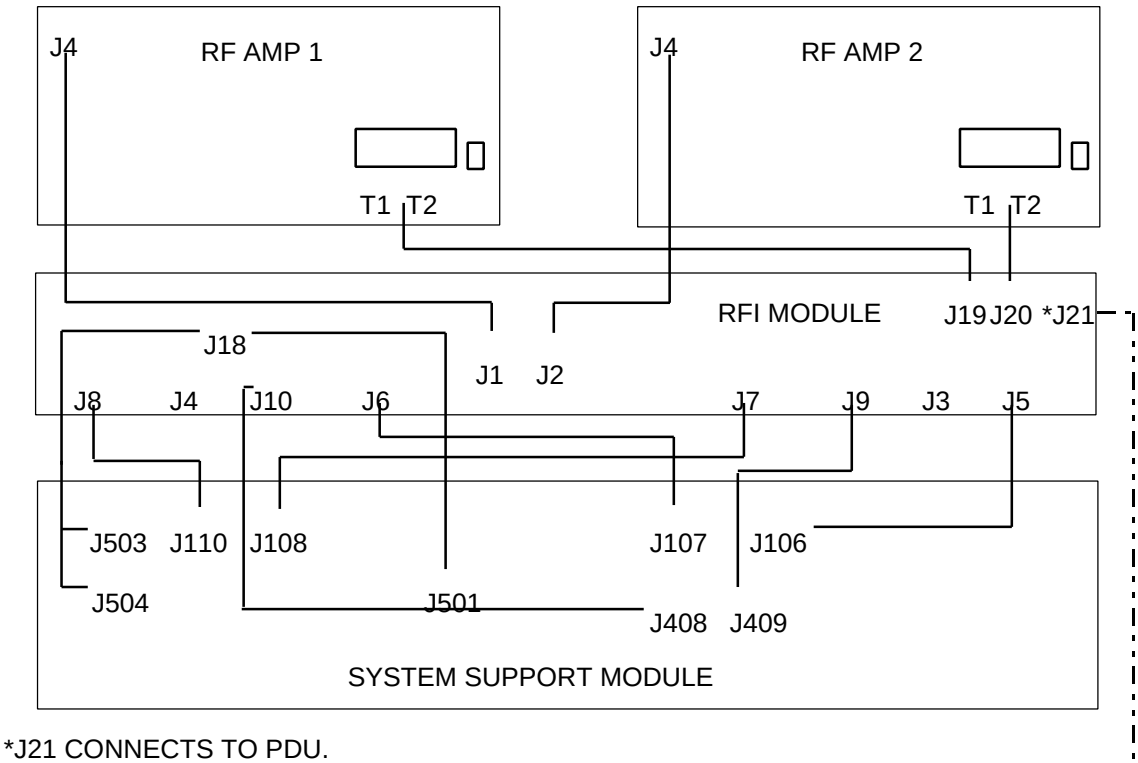
1- OVERVIEW

The 0.7T (GRFD) Power cabinet contains a solid state RF Amplifier, a RF Interface (RFI) module, the System Support Module (SSM), the gradient subsystem and the PDU. This section provides the theory of operation of the System Support Module.

The RFI (RF Interface module) consists of four modules; Input conditioning module, Output module, Interface Translator module and a commercially available power supply. The RFI functions as an interface between the SSM and the RF Amplifier with each module performing functions associated with its title.

The SSM behaves slightly differently depending on the cabinet installation. While several cabinet configurations use the same SSM hardware, the interpretation of MDS (Multi-Drop Serial Link) commands, the standard for communications with the SSM, depends on the peak power of the RF Amplifier and must be configured accordingly. This configuration ensures compatibility between the MDS commands and the RF Amplifier type. The 0.7T (GRFD) Power Cabinet uses the 0.7T RF Amplifier, which has a peak power of 9 kW (body mode). Service procedures have been included in this documentation which allow configuration using the front panel switches or using an external laptop computer.

A block diagram showing the cabinet cabling interconnection is shown in Illustration 1-1. Most of the external cables connect directly to the SSM. If the SSM must be extended from the rack, these cables will have to be extended with the module. The cables have enough slack to allow extension of the SSM. In some sites, the positioning of these cables prohibits this extension. For this reason, most procedures involving SSM adjustments, maintenance, and diagnostics can be performed using test-points and controls accessible on the outside of the module.

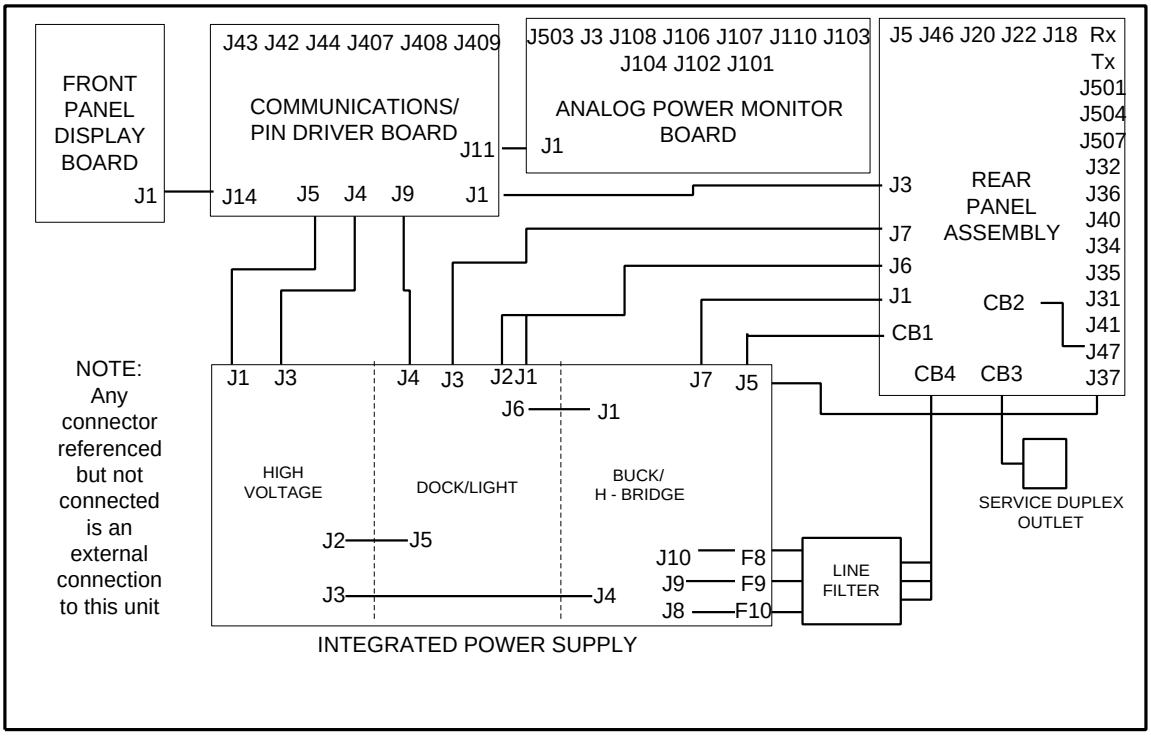


*J21 CONNECTS TO PDU.

SSM REAR CABLE INTERCONNECTS
ILLUSTRATION 1-1

1-1 System Support Module (SSM)

1. Illustration 1-2 contains a block diagram of the SSM and its external interface. In summary, the SSM provides seven general functions:



SYSTEM SUPPORT MODULE EXTERNAL INTERFACE FUNCTIONAL BLOCK DIAGRAM
ILLUSTRATION 1-2

A. a collection of the power supplies used throughout the MRI system

B. power supply test points

C. amplitude gain envelope feedback (this function is not used with the 0.7T Power Cabinet)

D. digital fault monitoring, control, and diagnostics

E. a front panel interface for configuration and performance monitoring

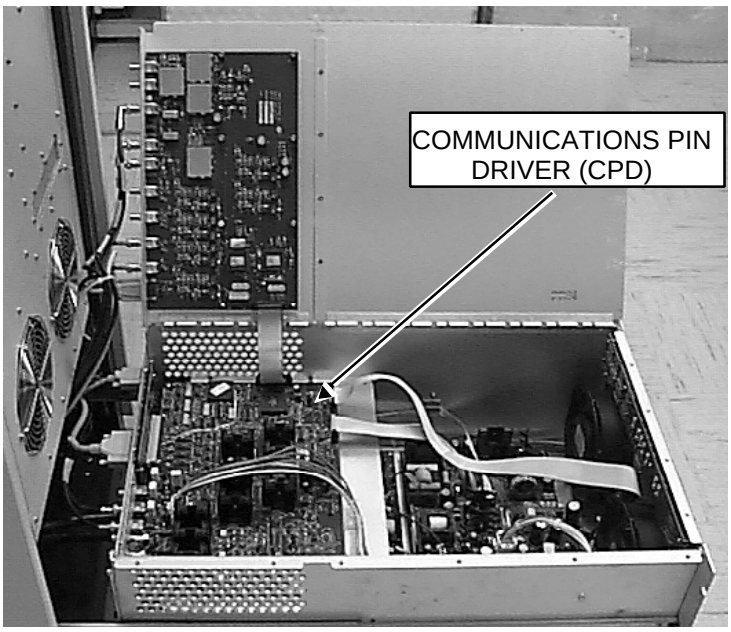
F. firmware which decodes the Multi-Drop Serial (MDS) bus at address $00

G. a RS-232 port with an instruction set to assist servicing

2. These functions are distributed among five field-replaceable units (FRU's) as follows:

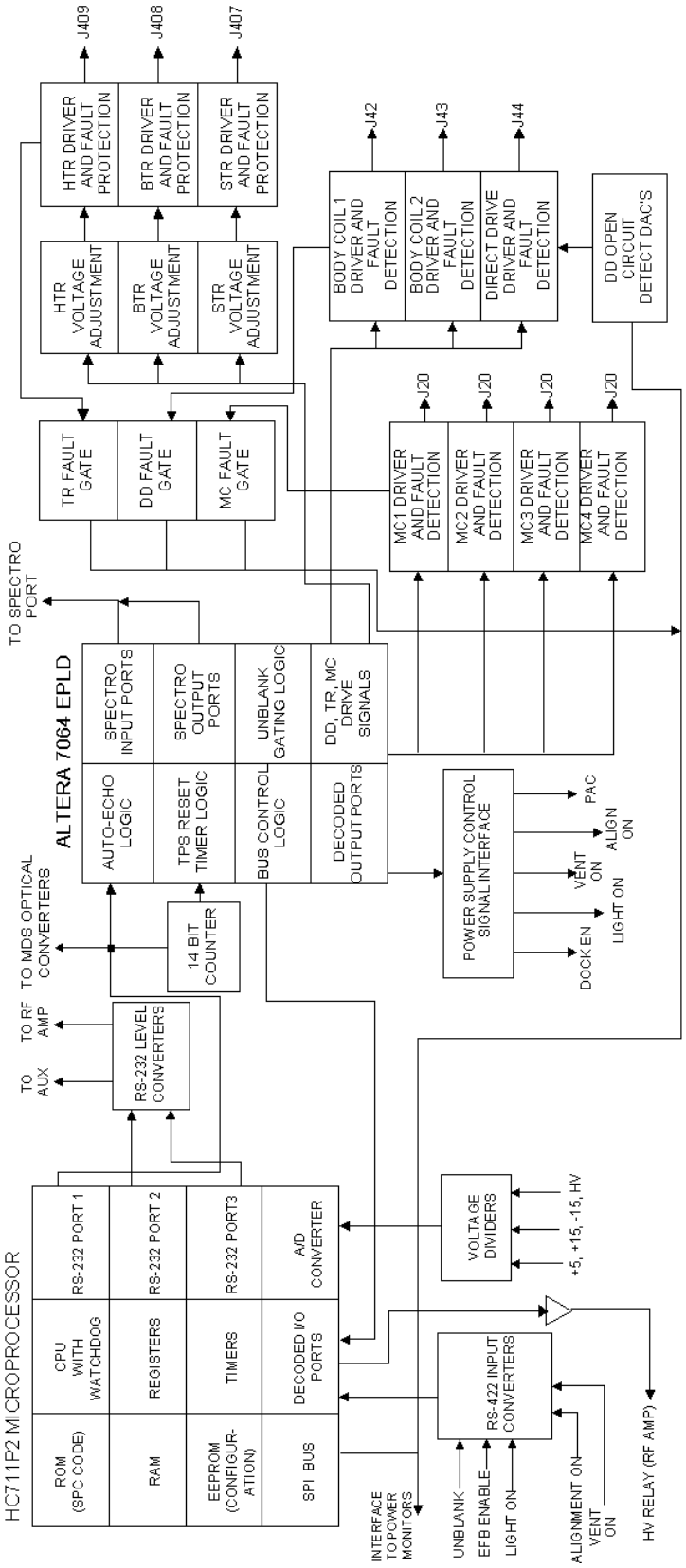
1-1-1 Communications Pin Driver (CPD)

See Illustration 1-3 and Illustration 1-4. This module is a printed circuit board (PCB) mounted on a sheet metal base plate. The PCB includes circuitry for the TR, DD, body coil (Body 1 and Body 2), and multicoil bias supplies. It includes all of the digital logic associated with driver fault detection as well as the interfaces to the amplifier power monitors, the power monitors, the MDS, and the auxiliary serial ports. The digital logic on the CPD includes a highly integrated 68HC11 series microprocessor that contains the software associated with the MDS and auxiliary serial ports. It also includes an Altera EPLD that contains all the logic associated with driver control.



COMMUNICATIONS PIN DRIVER LOCATION
ILLUSTRATION 1-3

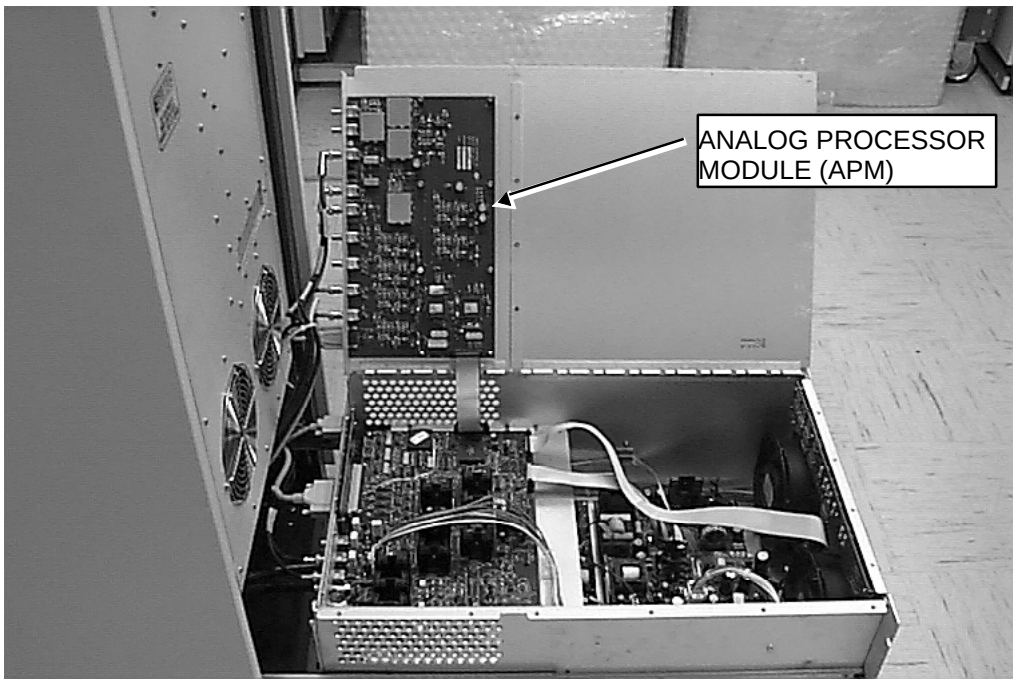
1-1-1 Communications Pin Driver (CPD) (continued)



COMMUNICATION PIN DRIVER - FUNCTIONAL BLOCK DIAGRAM
ILLUSTRATION 1-4

1-1-2 Analog Processor Module (APM)

See Illustration 1-5 and Illustration 1-6. This module is also a PCB mounted on a sheet metal base plate. It contains all of the circuitry associated with the two (redundant) RF power monitors (0.7T uses Head and Body).

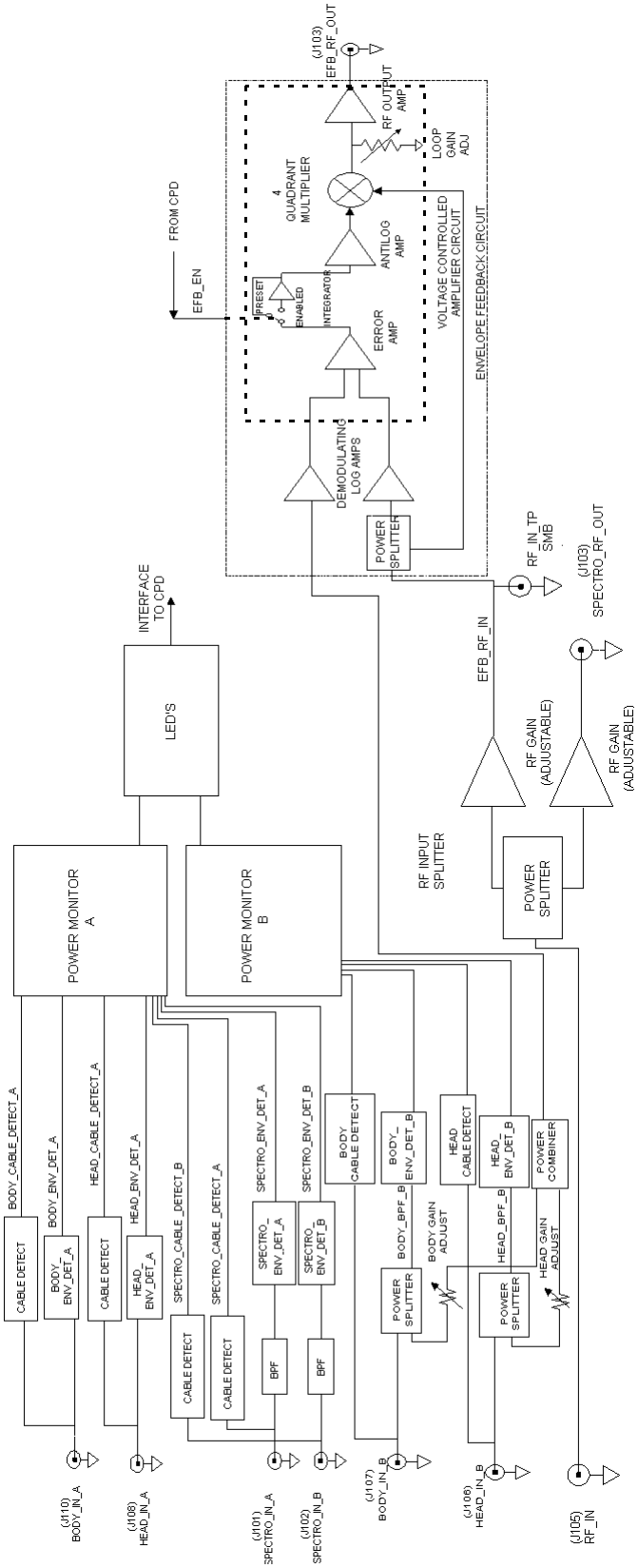


ANALOG PROCESSOR MODULE LOCATION
ILLUSTRATION 1-5

Note

The envelope feedback function is not used with the 0.7T GRFD Power Cabinet.

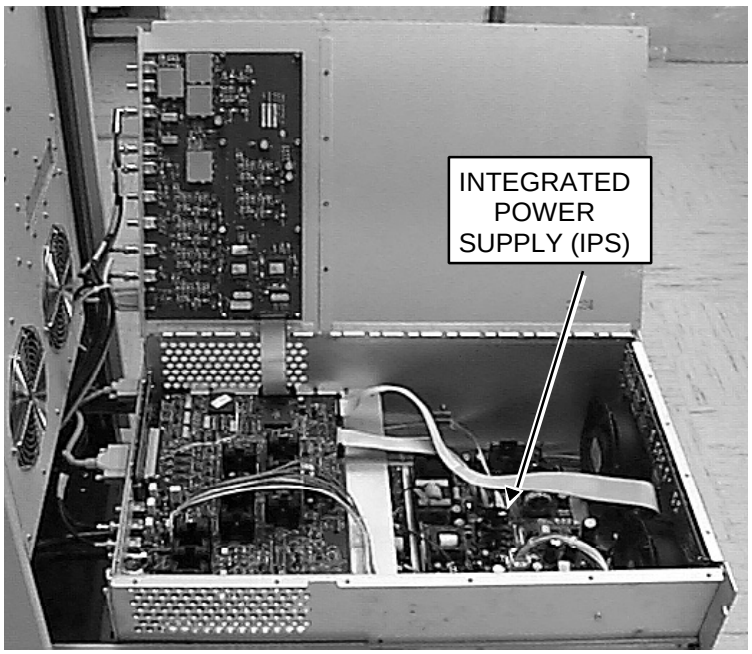
1-1-2 Analog Processor Module (APM) (continued)



ANALOG POWER MONITOR - FUNCTIONAL BLOCK DIAGRAM
ILLUSTRATION 1-6

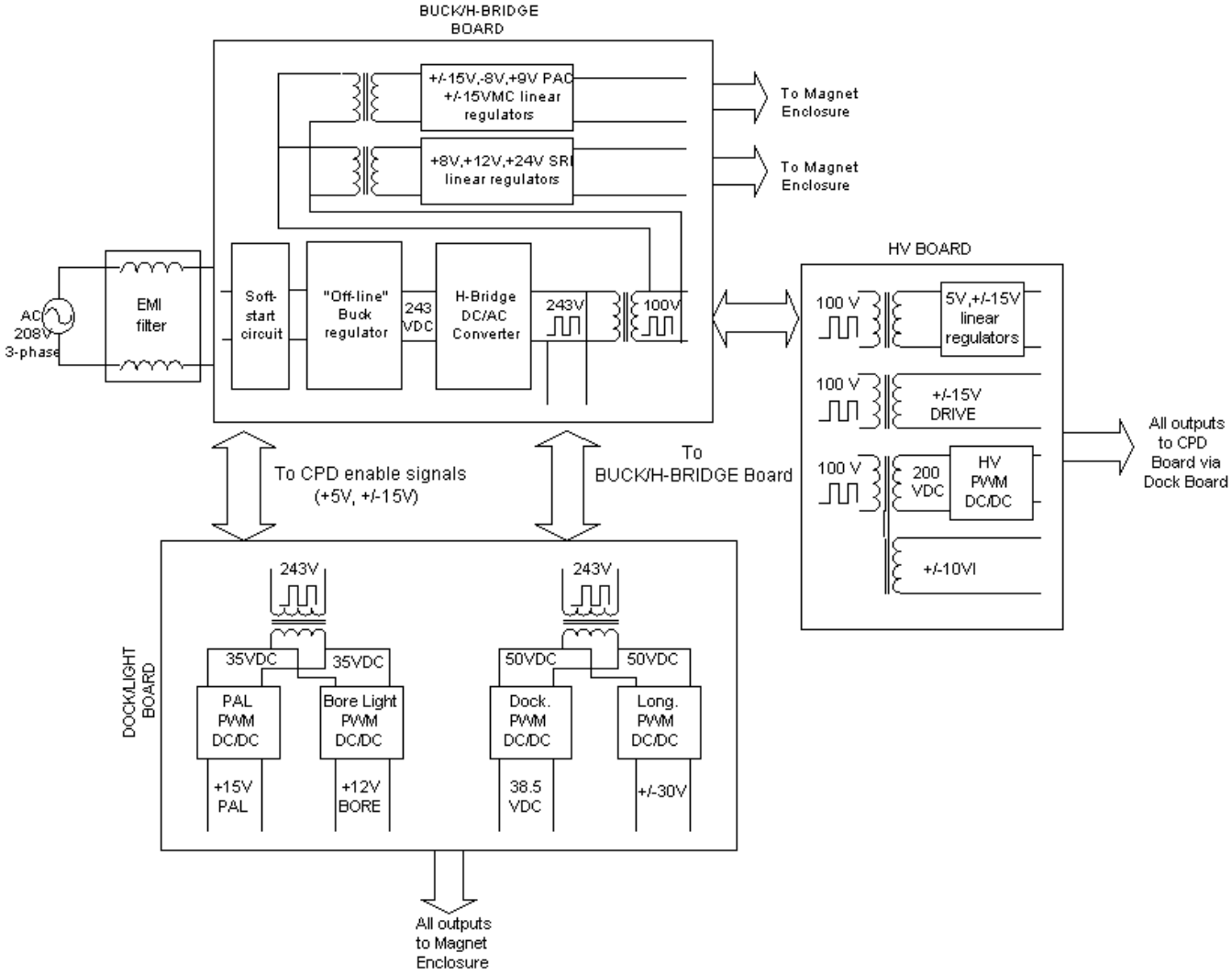
1-1-3 Integrated Power Supply (IPS)

See Illustration 1-7 and Illustration 1-8. This module contains three boards mounted on a single piece of sheet metal. It generates the PAC, SRI, light, and docking supplies, as well as those used within the System Support Module. It includes all wiring internal to the IPS.



INTEGRATED POWER SUPPLY LOCATION
ILLUSTRATION 1-7

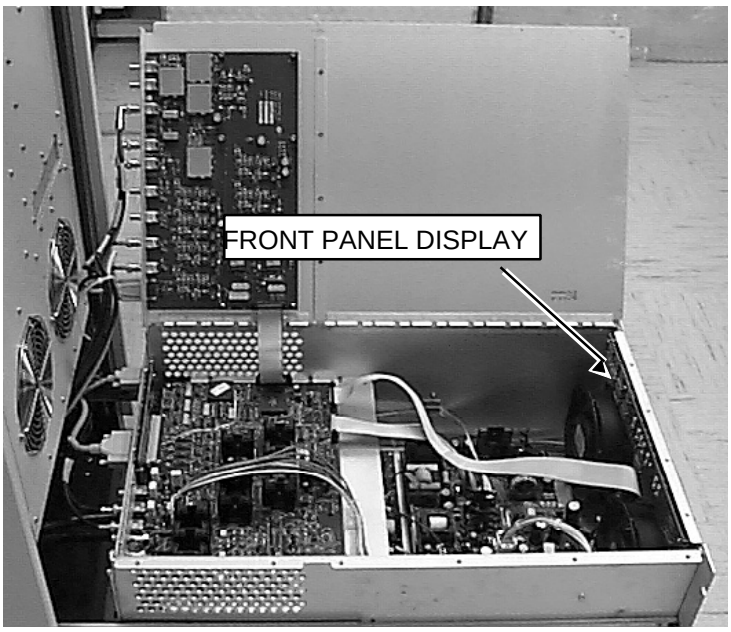
1-1-3 Integrated Power Supply (IPS) (continued)



INTEGRATED POWER SUPPLY - FUNCTIONAL BLOCK DIAGRAM
ILLUSTRATION 1-8

1-1-4 Front Panel Display

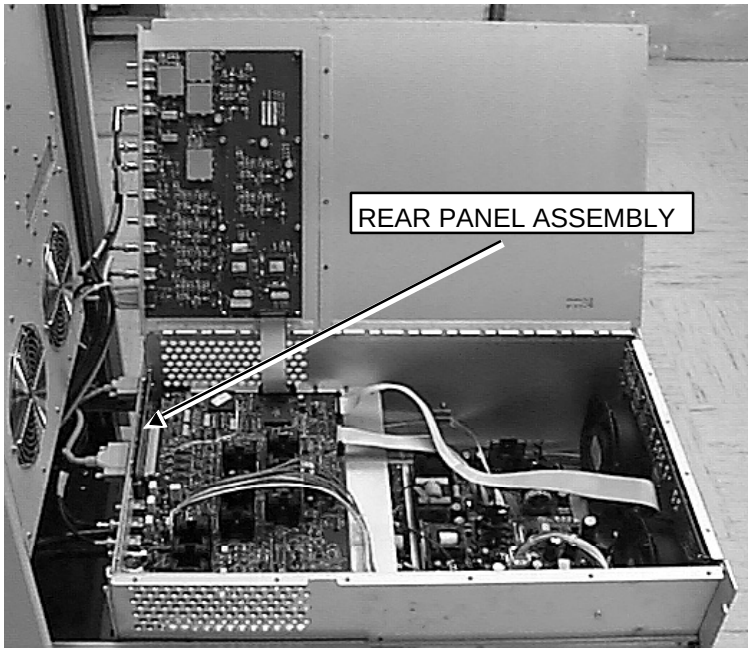
See Illustration 1-9. This module is a single PCB mounted in the front of the module. It includes circuitry that drives many LEDs and detects the positions of control switches. It also detects the presence of the front door.



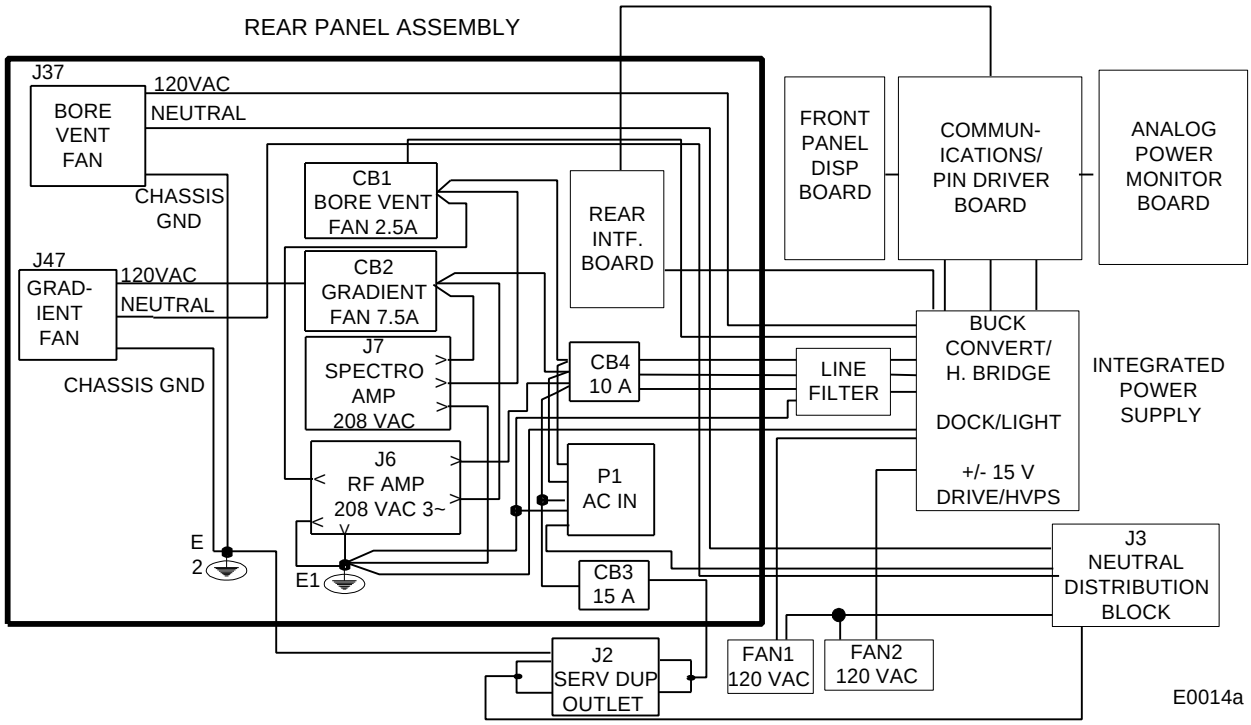
FRONT PANEL DISPLAY LOCATION
ILLUSTRATION 1-9

1-1-5 Rear Panel Assembly

See Illustration 1-10 and Illustration 1-11. This module contains the rear interface PCB mounted on a sheet metal plate combined with the circuit breakers, the ac connectors, and some of the ac power distribution wiring.



REAR PANEL ASSEMBLY LOCATION
ILLUSTRATION 1-10



REAR PANEL ASSEMBLY - FUNCTIONAL BLOCK DIAGRAM
ILLUSTRATION 1-11

1-2 Firmware

The firmware physically is located inside a MC68HC711P2 chip on the CPD board. The code can be viewed logically in three distinct tasks:

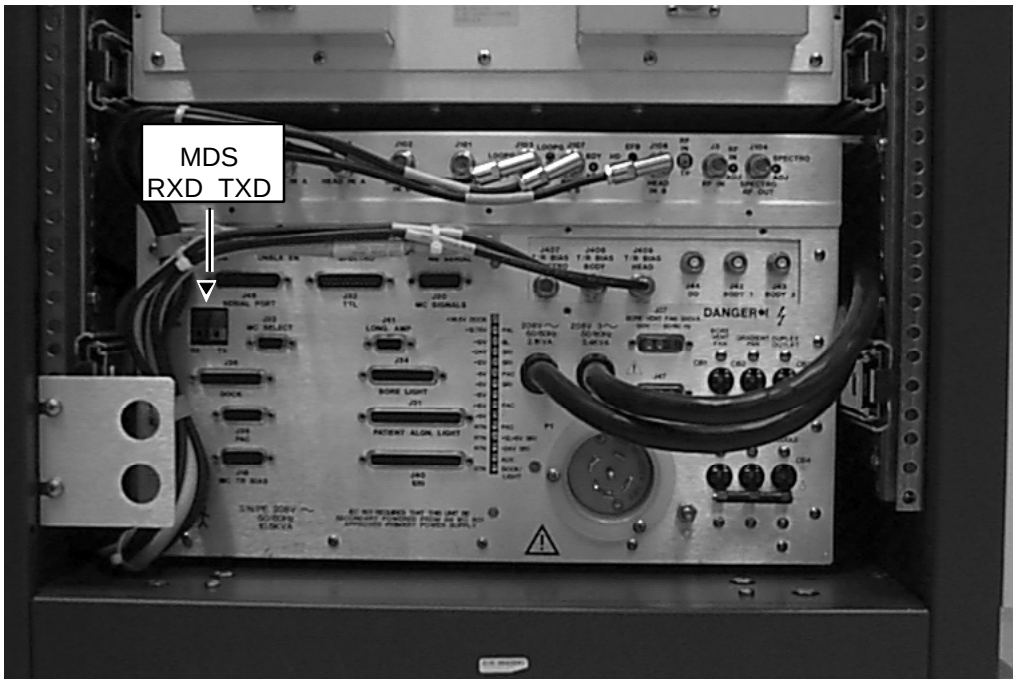
The MDS task decodes and executes instructions received over the optical cables. These instructions are limited to monitoring the normal safe operation of the cabinet and specific configuration commands.

The Aux task decodes and executes instructions received over the auxiliary RS-232 serial port. This instruction set includes all the commands necessary to control, monitor, and configure the RF circuitry.

The front panel task monitors the front panel switches and executes actions accordingly. Normally, this task performs only a monitoring service. However, special switch settings allow diagnostic testing also.

1-3 MDS

The protocol is 9 bit serial, 1 start bit, 1 stop bit, transferred at 9600 baud. The MDS connects to the cabinet as two fiber optic cables connected to the back of the cabinet as shown in Illustration 1-12. These signals are converted into electrical signals by HP transceivers located on the rear interface board. Because access to the PCB is difficult, test points TP4 (MDS_RXD) and TP8 (MDS_TXD) located on the CPD board contain the electrical signals RXD and TXD to assist in debugging, where RXD = incoming data and TXD = outgoing data.



MDS CONNECTION
ILLUSTRATION 1-12

MDS instructions allow:

- configuration of the drivers
- monitoring of the driver fault status
- configuration and monitoring of two independent power monitors
- control and monitoring of multicoil, DD, and body coil enables
- control and monitoring of the narrow band and broadband amplifiers

1-4 Aux

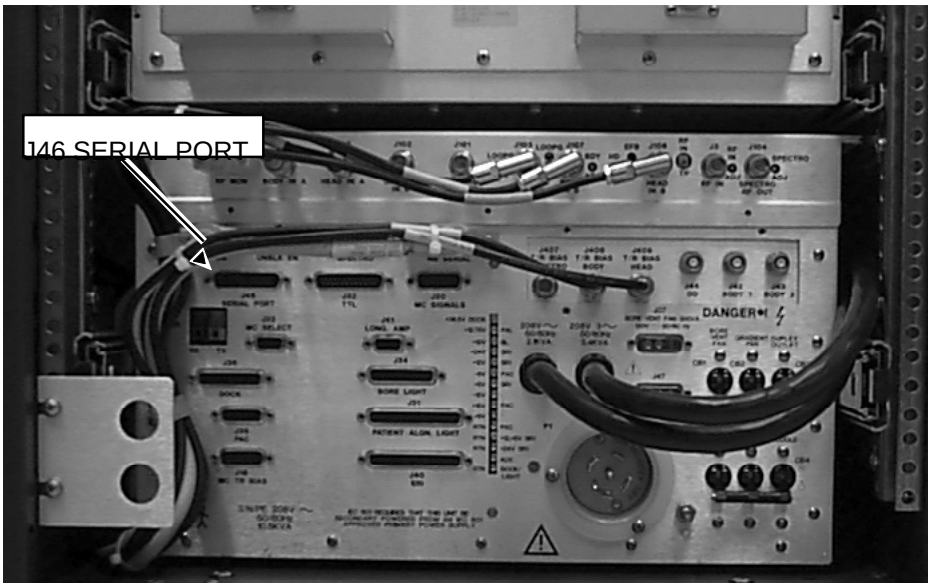
The Aux port is "standard" RS-232. The port is configured for 8 data bits, 1 start bit, 1 stop bit, and no parity. Data is transferred at 9600 baud. The instruction set is constructed from ASCII characters with all commands ending in Carriage Return (0x0d). All commands result in some return message. This message always ends in Line Feed (0x0a). The RF cabinet never sends a message without being asked first. This simplifies the interfacing code requirements.

The Aux port is configured as a DTE (Data Terminating Equipment) device and uses a minimal hardware handshake to transfer data. Computers are typically DTE devices and consequently, a cable signal interchange is needed at J46 (see Illustration 1-13) to interface the RF cabinet to most computers. Illustration 1-14 shows a null modem (no handshake) adapter with the required signals, or these signals are available through the use of the serial port interface cable (part number 216-0200-38), which is shipped with every 0.7T GRFD Power cabinet.

Aux (RS-232) instructions allow:

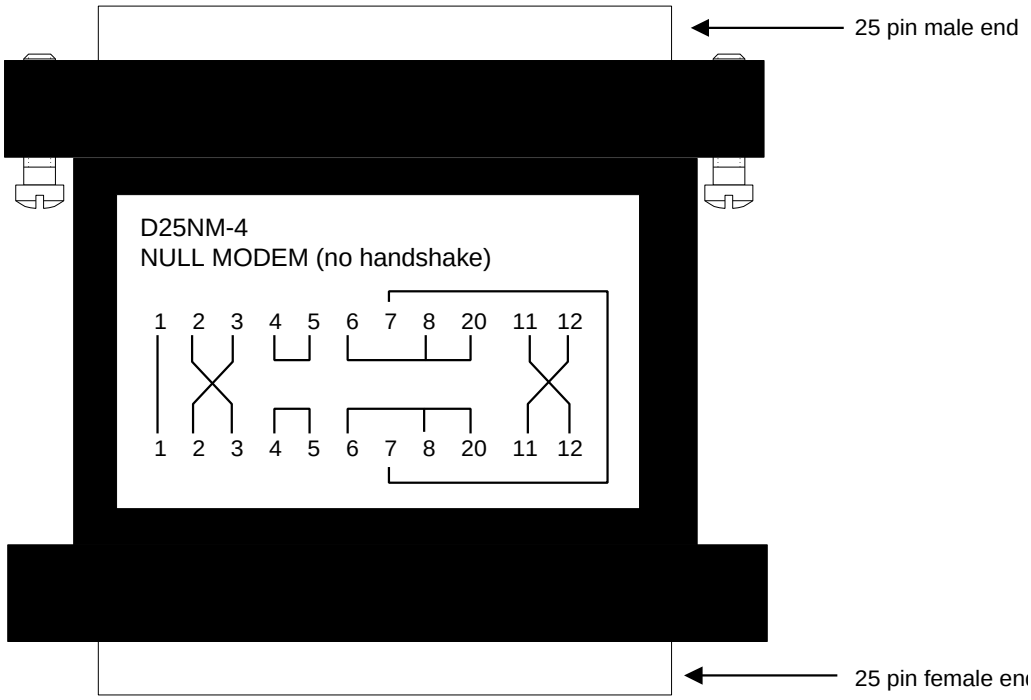
- configuration of the drivers
- monitoring of the driver fault status
- configuration and monitoring of two independent RF power monitors
- control and monitoring of multicoil, DD, and body coil enables
- control and monitoring of the narrow band and broadband amplifiers
- changing configuration parameters
- reading and writing the various address busses
- reading and writing the safety power monitor parameters
- reading the front panel switch positions

Laptop diagnostic software has been provided which interfaces to the Aux port and is supported by Erbtec.



AUX CONNECTION
ILLUSTRATION 1-13

1-4 Aux (continued)



NULL MODEM (NO HANDSHAKE) ADAPTER
ILLUSTRATION 1-14

1-5 Front Panel Display

During normal operation, the front panel display contains a collection of twelve discrete LEDs, which indicate the status of the power monitors and certain possible fault conditions. With the exception of the "sense" LEDs, these should all be off during normal operation. In addition to the discrete LEDs, the front panel contains two bar LEDs containing 10 lights each. These are located behind a translucent red plastic cover. Each of these lights indicates a specific RF circuit fault or warning. In normal operation, all of these lights should also be off. The detailed definitions of the LEDs and the associated switches are described in the section 6 - Front Panel Interface.

2- COMMUNICATIONS PIN DRIVER (CPD)

See Illustration 1-4. The CPD contains ten different bias drivers and their associated fault detection circuitry. The drivers can be grouped in three categories as shown:

TR drivers:
Head TR: +8.0 VDC during unblank (transmit), –12V during blank (receive)
Body TR: +4.0 VDC during unblank (transmit), –12V during blank (receive)
MNSpectro TR: Not Applicable

DD/Body coil drivers (1.5T/1.0T):
Dynamic disable: +1000V/+500V or –2.0A current regulated
Body coil 1: +1000V/+500V or –1.1A current regulated
Body coil 2: +1000V/+500V or –1.1A current regulated

Multicoil drivers:
MC1: +5V or –5V (enabled by software)
MC2: +5V or –5V (enabled by software)
MC3: +5V or –5V (enabled by software)
MC4: +5V or –5V (enabled by software)

The purpose of the driver section of the CPD board is to individually select the different system coils and to provide the distinction between transmit and receive modes on these coils by biasing PIN diodes located at the coils (or in the associated TR Switch) to either pass or prohibit the flow of RF energy.

Pulsed drive signals (amplifier unblank signals) are directed to the various drive elements: Multi-coils, TRs, DD, and body coil drivers, as specified by the communications section of the CPD board. Additionally, open-circuit (monitored during transmit mode, current flow is not adequate) and short-circuit (monitored during receive mode, negative receive mode value is less than –10 VDC, ±0.5 VDC) error detection signals (faults) for each of the drivers are stored in fault buffers which are read via select lines originating from the CPD microprocessor. The CPD board reports any faults to the remainder of the system where appropriate actions are taken.

The Multi-coil drivers consist of four separate drivers that each output a voltage of ±5 volts at nominally 0.5 amp of current. Each driver receives its own drive signal from the EPLD. The drive signal goes through a level shift circuit consisting of a comparator and dual rail precision line driver to obtain +5V and –5V levels. A high power operational amplifier (op-amp) accurately converts the low-current ±5V drive level to a high-current ±5V level. External circuitry around the op-amp determines its gain and frequency response and sets current limits to 1 amp.

A low value precision current sense resistor and high gain instrumentation amplifier accurately measure the output current of the op-amp. A window comparator arrangement triggers a fault signal if the measured value of current does not fall within a small, precise range.

2- COMMUNICATIONS PIN DRIVER (CPD) (continued)

By keeping tight control of the 5V supply source (calibrated on the integrated power supply HV board) and using precision tolerance components, it is possible to meet the stringent open-circuit and short-circuit fault detection requirements. Open and short-circuit coil detection is based on small changes in the level of output current. Typically, 0.5 amp of current is drawn by the multicoil loads. If greater than 0.55 ± 0.02 amp is drawn, a short-circuit fault is to be reported. If less than 0.45 ± 0.02 amp of current is drawn, an open circuit fault is to be reported. The limits of the window comparator change polarity with a change in polarity of the drive signal. The effect is such that when an open circuit condition is being evaluated, a short circuit fault is forced, and when a short circuit condition is being evaluated, an open circuit fault is forced. Thus, the error-detection circuitry is essentially constantly testing itself. All multicoil faults are presented to the inputs of a buffer IC. The microprocessor polls the faults by sending an enable signal to the buffer within approximately 225 microseconds from the system unblank edges.

The output drive signals pass through RF T-type filters, used to limit the amount of RF energy entering or leaving the circuit board (in the form of conducted/radiated switched power supply harmonics or scan frequency energy).

The TR drivers consist of a head, body, and spectro (Multi-Nuclear Spectroscopy, not used) driver, which output levels of 8 volts, 4 volts, and 4.3 volts, respectively, during system unblank and approximately –12 volts during system blank (as referenced to ground). The TR driver outputs enter their respective RF coupler in the RFI. In the coupler, they are low-pass filtered and combined with the amplifier RF output as a DC offset.

A single TR drive signal originates from the EPLD and is used by all three TR drivers. The polarity of this signal defines the voltages on a summing amplifier circuit containing the same type of high power op-amps used for the Multi-coil driver circuits. Each of the three summing amplifier circuits contains a potentiometer so the voltage level of the resultant high output pulse can be adjusted. When the TR drive signal is low, the summing node on each of the three amplifier circuits is identical and forces the output to approximately –12V.

External circuitry around the op-amp determines its gain and frequency response and sets current limits to approximately 4 amps for the body TR driver and 2.5 amps for the head and spectro (MNS) drivers. Similar to the Multi-coil driver circuits, low value current sense resistors and high gain instrumentation amplifiers measure the output current of the op-amps for open-circuit fault determination. For each of the TR circuits, a current measurement below 0.5 amp represents an open-circuit fault condition. Short-circuit fault determination is achieved by sampling the level of receive-mode voltage (~–12V) and comparing that level to –10V. If greater than –10V, a short-circuit fault is to be reported. All TR faults are presented to the inputs of a buffer IC. The microprocessor polls the faults by sending an enable signal to the buffer within approximately 225 microseconds from the system unblank edges.

During receive mode, when the outputs are –12V, a diode on the output of each driver forces a resistor in series with the output. This resistor limits the current draw to 300mA, protecting sensitive electronics on the load end.

Like the Multi-coil drivers, the TR drive outputs pass through RF T-type filters, which limit the amount of RF energy entering or leaving the circuit board.

2- COMMUNICATIONS PIN DRIVER (CPD) (continued)

The body 1, body 2, and DD drivers provide 500V or 1000V to their loads when the system is in body mode, or act as 2 amp (body 1 and body 2) and 1 amp (DD) current sinks while the system is in head mode.

Like the TR drivers, a single drive signal originates from the EPLD and controls all three drivers. The drive signal either disables the current sink loops and turns on the high voltage transistor, or turns off the high voltage transistor and enables the current sink loops. The high voltage transistor is driven by an optically coupled, high-current, transistor driver. The rails of the optical driver are an isolated ±10V supply. This supply and the 500/1000V supply originate from the HV board located on the integrated power supply. The isolated ±10V supply will be dc offset by up to 1000V when the high voltage transistor is on. Selection of 500V or 1000V is made by the positioning of a jumper on the HV board. The jumper should be positioned for 500V in the 1.0T systems.

When the drive signal is such that the high voltage transistor is in an off state, the current-sink loops will be enabled. When the loops turn on, current flows through the transistors and across sense resistors. The voltage developed across the sense resistors is buffered and feeds a summing amplifier. A voltage of approximately 1V is needed across the sense resistor in order to satisfy the summing op-amp circuitry. If < 1V appears across the sense resistor, the summing op-amp output rises, allowing more voltage onto the gates of the sink transistors, and thus more current flows through the transistor. If > 1V appears across the sense resistor, the summing op-amp output falls, allowing less voltage onto the gates of the sink transistors, and thus less current flows through the transistor. A value of 1V across the sense resistor defines a current of 2 amps for the body coil drivers and 1 amp for the DD driver.

The path of the drive signals to the current loops and the high voltage transistor is delayed in such a manner as to cause both the sink loops and the high voltage transistor to turn on slowly and turn off quickly. This prevents the possibility of both the current loops and the high voltage transistor being on at the same time.

Short-circuit fault detection is activated when significant current is drawn when sourcing 500V or 1000V (body mode). The short-circuit detector consists of an optical coupler connected across a sense resistor in series with the output. Approximately 20mA of current are required to turn on the coupler and signal a fault. After initial charging of the load capacitance (within ~50 microseconds of unblank), future activation of the coupler will represent a fault condition.

Open-circuit fault detection involves monitoring the output voltage when the sink loops are activated. A drop in output voltage (1-2 volts less than nominal) signals an open circuit condition. Calibration of the open-circuit detection threshold is an automated procedure. When calibration is performed, the microprocessor controls a D/A converter that adjusts the threshold on the open-circuit detect comparator until a fault is recorded. Afterward, the microprocessor reduces the adjustment by a number of bits corresponding to ~1-2 volts.

All body coil and DD open and short-circuit faults are presented to the inputs of a buffer IC. The microprocessor polls the faults by sending an enable signal to the buffer within approximately 225 microseconds from the system unblank edges.

3- ANALOG PROCESSOR MODULE (APM)

The APM performs: the amplitude linearization of the RF power amplifier utilizing envelope feed back (EFB), the redundant power monitor envelope detection and scaling functions. See Illustration 1-5 and Illustration1-6.

3-1 Envelope Feedback (EFB)

EFB is a function of the SSM but is not used in the 0.7T (GRFD) Power Cabinet.

4- INTEGRATED POWER SUPPLY (IPS)

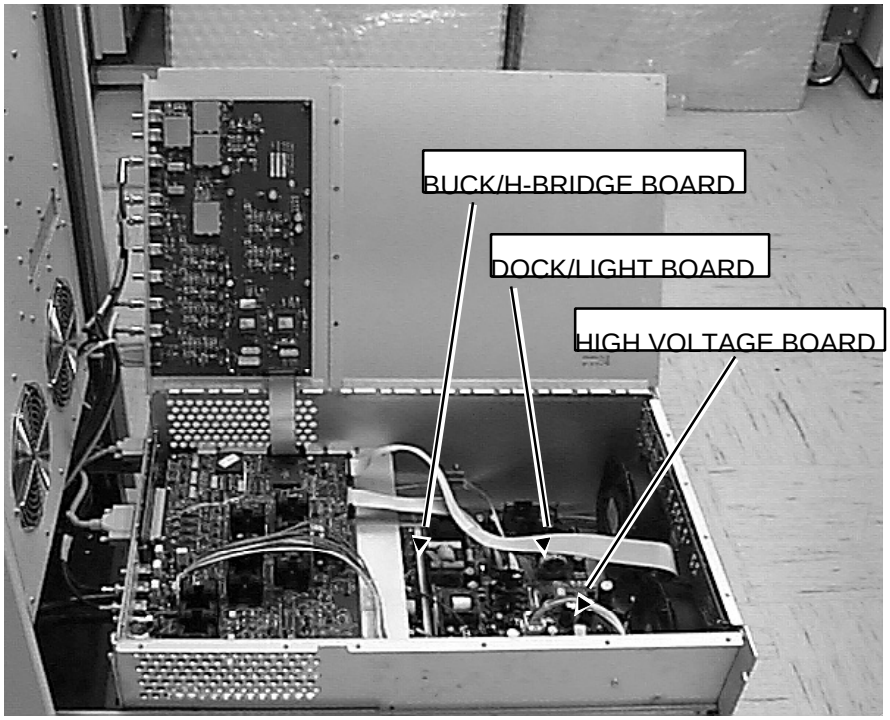
CAUTION

There are no ground reference points on the IPS to reference.
Do not reference any point on the IPS with a grounded oscilloscope.

The IPS, located in the system support module (SSM) of the cabinet, is the power source for the following:

- Communications pin driver (CPD) board within the SSM
- Analog power monitor (APM) within the SSM
- Physical acquisition controller (PAC) located within the magnet shroud
- Scan room interface (SRI) located within the magnet shroud
- Bore and patient alignment lights (PALs) located within the magnet shroud
- Longitudinal and docking motors located within the scan room

The IPS consists of three circuit board assemblies: the buck/H-bridge, the high voltage, and the docking/light (dock/light). See Illustration 4-1 and Illustration 1-8.



IPS THREE CIRCUIT BOARD ASSEMBLIES
ILLUSTRATION 4-1

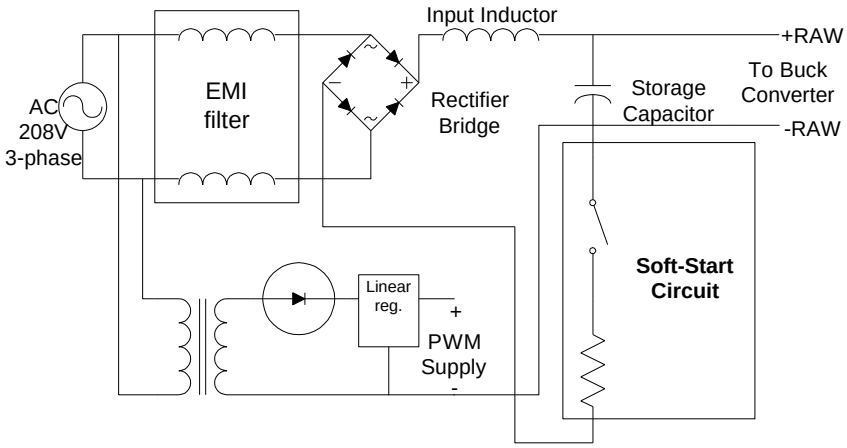
4-1 Buck/H-Bridge Board

CAUTION

Do not reference any point on the IPS with a grounded oscilloscope.

The buck/H-bridge board contains the primary power conversion circuitry for all of the power supplies as well as the output circuitry for the PAC, SRI, and Multi-coil supplies. Input power, in the form of 3-phase, 208 ± TBD Vac is input to the PCB after passing through an off-board EMI line filter. The 3-phase ac voltage is rectified and low pass filtered through an inductor into shunt storage capacitors. The charging of the input storage capacitors is controlled by a pulse-width-modulator (PWM) in-rush limiting circuit designed to limit the level of current flow into the power supply. The PWM is designed to run such that its transistor switching element is always full on if less than 10 amps of current is flowing through the transistor. If more than 10 amps of current flows through a sense resistor in series with the switching transistor, the drive to the switching transistor is interrupted. The action of the in-rush limiting circuit works both to limit the amount of in-rush current into the storage capacitors on power up and to set an upper limit of power input to the entire supply (~3000W).

Directly off of the ac line, two voltage phases are connected to a step down transformer, the output of which is rectified, filtered, and used to power a 15V regulator circuit. This 15V, referenced to the lower potential raw voltage on the storage capacitors, is used to power the buck and H-bridge PWM converter ICs as well as supporting enable and sense circuitry. See Illustration 4-2.

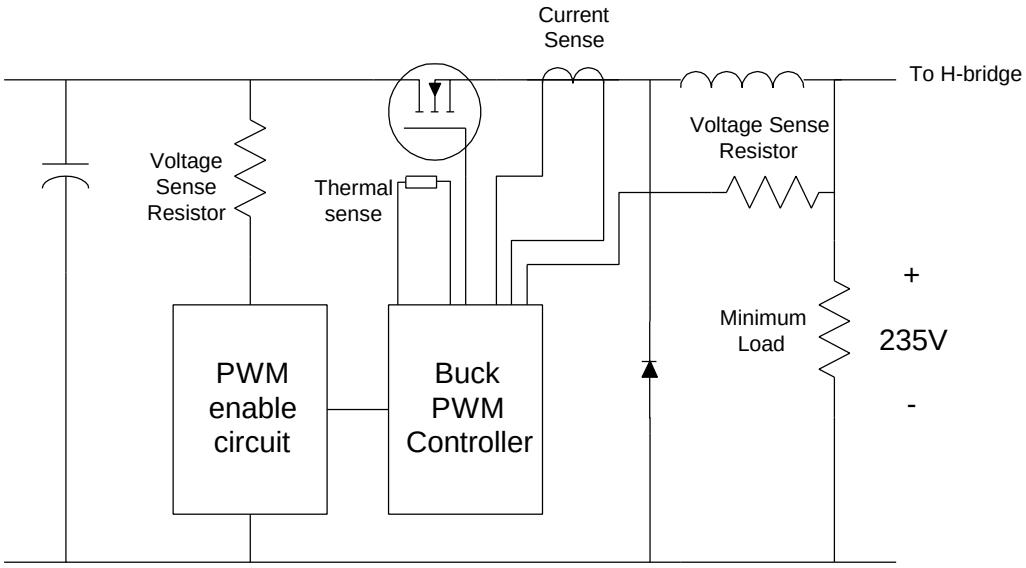


INPUT CIRCUIT BLOCK DIAGRAM
ILLUSTRATION 4-2

4-1 Buck/H-Bridge Board (continued)

A buck topology dc/dc current-mode PWM converter is used to obtain a regulated voltage of 235V from the raw dc voltage appearing across the main input storage capacitors. 235V was chosen because it is the highest value that can be regulated when PWM efficiencies and line variation are considered. The action of the buck converter is impeded until sufficient voltage appears at the storage capacitors such that regulation at 235V is possible. This is accomplished via a PWM enable circuit that senses the raw voltage on the storage capacitors and compares it to a given threshold that, in turn, enables the buck PWM IC. Hysteresis is built into the PWM enable circuit so that the buck PWM IC is not disabled until the raw voltage is far below the level required for normal operation (but not so low as to require excessive current flow). This hysteresis is necessary so that the voltage drops in the raw voltage due to current loading of the supply (both steady state and transitory in nature) do not cause premature shutdown of the regulator.

The buck regulator generates a regulated voltage preset to 235V by the manufacturer. This voltage appears across a 2500-ohm minimum load (for converter regulation purposes) and the switching elements of the H-bridge. A transformer coupled BJT and JFET drive circuit for the main switching transistor allows for fast turn-on and turn-off times, improving the overall control of the circuit. The buck converter monitors the output current through the main switching transistor, via a current sense transformer, for both regulation and maximum current limit considerations. The current limit is set at approximately 8 amps (~2000 W). An outer sense loop monitors the output voltage via a resistor divider for the purpose of voltage regulation. The buck PWM IC is designed to operate at approximately 25kHz with duty cycles approaching 100% and efficiencies over 90%. Thermal sensing of the buck PWM switching transistor heatsink is used as an added precaution against over-current. See Illustration 4-3.

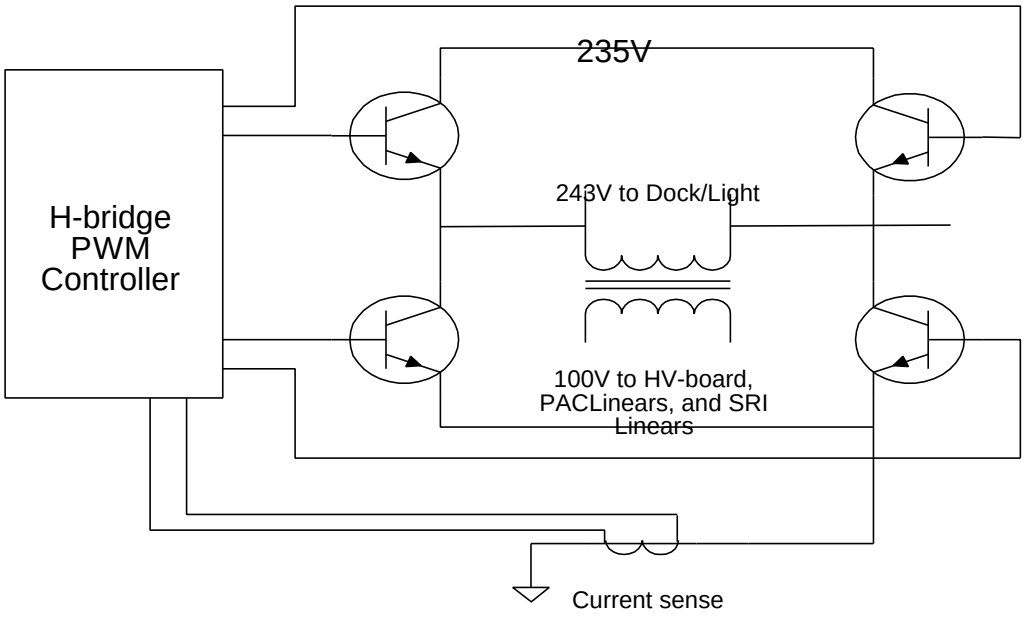


BUCK CIRCUIT BLOCK DIAGRAM
ILLUSTRATION 4-3

4-1 Buck/H-Bridge Board (continued)

The purpose of the H-bridge circuit is to convert the regulated 235V into a switched voltage suitable for efficient down conversion through step-down transformers. The H-bridge is a dc/ac PWM converter run open loop with respect to voltage. This converter produces a 25kHz square wave of 243V amplitude. The H-bridge converter also monitors the output current through the switching elements, via a current sense transformer, for maximum current limit considerations. The current limit for the H-bridge is set at approximately 10 amps. Voltage feedback via a resistor divider serves only to shutdown the regulator in the event of an over voltage condition (243V rising above ~260V). The H-bridge converter is always enabled, requiring only the IC supply voltage for operation.

The switched output waveform from the H-bridge travels to two different destinations. First, it proceeds directly to the dock/light board and its associated higher power needs (docking and longitudinal motors, PALs, and bore lights). Second, it passes through a transformer where it is stepped down to 100V and feeds SRI and PAC supply circuits on the buck/H-bridge board and CPD supply circuits on the high voltage board. See Illustration 4-4. The PAC and SRI circuits on the buck/H-bridge board consist of step-down transformers, bridge rectifiers, input filters, and linear regulators. Because the 100V is constant (because it originates from the regulated 243V), the step-down transformers are designed such that the secondary voltages are only about 3-4 volts above the desired regulator output voltages when they reach the input to the regulators. This minimizes the voltage drop across the regulators and thus the power dissipated by the regulators. Input filters to the regulators are required because the rectified waveform contains a voltage dead-time as a result of the non-conduction period associated with the switching of the H-bridge converter. This dead-time is necessary to prevent possible cross-conduction of the switching elements in the H-bridge. Sizing of the filter components determines the amount of inductor current ripple and capacitor voltage ripple allowed at the input of the regulator. The PAC and ± 15V Multi-coil supplies share a common transformer, and the SRI supplies share a second transformer.



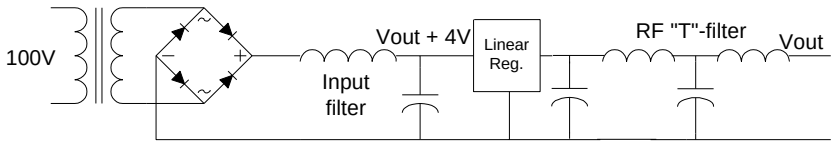
H-BRIDGE CIRCUIT BLOCK DIAGRAM
ILLUSTRATION 4-4

4-1 Buck/H-Bridge Board (continued)

The transformer feeding the PAC and Multi-coil circuitry serve seven linearly regulated supplies:

+15V @ 0.8A (PAC)
–8V @ 0.4A (PAC)
–15V @ 0.4A (PAC)
+8V or +9V @ 2.5A (PAC)
+15V @ 1A (multicoil), and
–15V @ 0.5A (multicoil).

(By way of an optically coupled control signal originating from the CPD board, the +9VPAC output can be switched between +8 and +9 volts by controlling the amount of adjustment current on the linear regulator.) The transformer feeding the SRI circuitry serves three linearly regulated supplies: +8V @ 2A, +12V @ 2A, and +24V @ 2A. The PAC, SRI, and Multi-coil supplies all leave the buck/H-bridge board via a connector to the rear interface board. On the rear interface board, RF filtering in the form of LCT filter assemblies is used to keep RF energy such as PWM switching harmonics from leaving the supply circuits. See Illustration 4-5.



TYPICAL LINEAR REGULATOR CIRCUIT
ILLUSTRATION 4-5

Additional wiring on the input power connector to the buck/H-bridge board routes fused current to the cooling fans in the front of the unit. These fans will be on whenever the main circuit breaker is turned on, regardless of whether or not any of the PWM converters are operating.

A solid state relay on the buck/H-bridge board directs ac power to the bore vent as directed by a digital signal originating from the CPD board and passing through the rear interface board.

4-2 High Voltage Board

CAUTION

Do not reference any point on the IPS with a grounded oscilloscope.

The high voltage board rests on top of the dock/light board and contains all the supplies necessary to power the CPD, APM, and front panel display. Its sole input from the buck/H-bridge board is the 100V switched waveform. This input travels to three step-down transformers. One of the transformer outputs feeds a set of three linear regulators in a similar fashion as the PAC and SRI circuits on the buck/H-bridge board. The stepped-down voltages are rectified, LC filtered, and connected to the inputs of linear regulators at voltages ~4V above the required regulator output levels. These linear regulated supplies of +5V@ 500mA and ±15V @ 500mA serve mainly as digital and low-current analog supply rails for the CPD, APM, and front panel display. These supplies are also locally RF filtered through LCT filter assemblies before they pass to the CPD board.

4-2 High Voltage Board (continued)

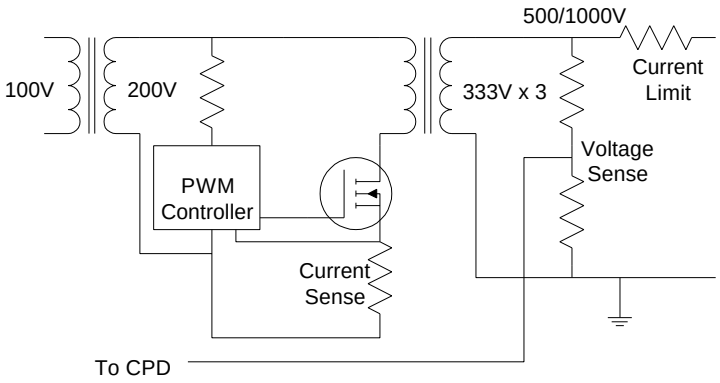
A second transformer provides high-current power for the CPD Multi-coil, TR, DD, and body coil drivers. The switched 100V is stepped down, rectified, and filtered to approximately ±15V. The filtering on these supplies is much greater because there is no linear regulator to help reject noise from the H-bridge switching dead-time. Local RF filtering in the form of discrete LC components helps to block RF energy from propagating to the CPD board.

The third transformer on the high voltage board is for the high voltage CPD supply and contains two secondaries, one step-up and one step-down. The step-up winding provides approximately 200Vdc after rectification and filtering. The 200V feeds a flyback topology, low power, current-mode PWM converter circuit. The other secondary provides a low-current dual voltage supply at ±10V. This supply contains no regulation (other than that provided by the input buck PWM) and contains only rectifier diodes, a RC filter, and output RFT filters. This supply has an isolated return that operates alternately between the level of the high voltage output and the high voltage return/common when in operation at the CPD board. The high voltage common, when the high voltage board is not mated to the CPD board, is referenced to chassis ground through a 750-ohm resistor.

The flyback converter consists of another transformer and a switching transistor. When this switching transistor is turned on, 200V appears across the primary of the output transformer, and current flow is established. When the switching transistor is turned off, current flow is interrupted, and current is transferred to the secondary of the output transformer. Approximately 335V is present on each of three secondaries on the output transformer, totaling 1000V at the output.

Power for the PWM IC is obtained by tapping off the 200Vdc bus through a current limiting resistor. Current sensing via a sense resistor, in line with the switching transistor, aids in control of the PWM IC and sets the current limit for the circuit to ~0.83 amps peak. A jumper configures the output to be either 500 or 1000V by selecting a different divider ratio for the output voltage. This divided-down output voltage is fed back to the PWM IC, where it is used to control the output switching duty cycle and thus, the output voltage. he voltage divider on the output also provides a means of discharge for the supply when powered down. The RC time constant for the discharge is approximately 13 seconds. A third divider ratio on the output voltage powers a sense signal, HV-SENSE, which provides the CPD with a means for determining the approximate voltage level of HV. An optically coupled, active low, enable signal from the CPD board allows the PWM IC to deliver output drive. The insertion of a second jumper bypasses the enable signal, allowing the PWM to operate without the CPD board. Peak current from the HV storage capacitors is limited to ~5 amps through an output current limit resistor. See Illustration 4-6.

4-2 High Voltage Board (continued)



HIGH VOLTAGE CIRCUIT BLOCK DIAGRAM
ILLUSTRATION 4-6

4-3 Dock/Light Board

CAUTION

Do not reference any point on the IPS with a grounded oscilloscope.

The dock/light board contains those supplies used for running the docking and longitudinal motors, as well as powering the bore and patient alignment lights. The power source for the dock/light board is the switched 243V waveform at the output of the H-bridge on the buck/H-bridge board. This voltage goes to two transformers; one powers the light supplies, and the other powers the motor supplies.

For the light circuits, the switched 243V is stepped down to approximately 35V, rectified, and filtered. The 35V then feeds two buck-mode topology switching power supply circuits. The two light PWM ICs have separate, active high, optically coupled enable signals originating from the CPD board. Both light circuits contain a current mode PWM controller IC, a main transistor switch element, and supporting gate drive and feedback/control circuitry. Power for the PWM ICs is obtained by tapping into the 35V dc bus through a current limiting resistor. The output voltage is monitored and fed back to the PWM circuits in one of two ways. First, if the feedback jumpers are installed in the outer voltage control loop, the nominal outputs will be controlled to +15V (PAL) and +12V (bore). Second, if the voltage feedback jumpers are removed, up to ~2V additional can be obtained (via pots in series with the PWM IC feedback control pin) to compensate for line loss. The PAL PWM IC is capable of higher output duty cycles (<100%) than the bore light PWM IC (<50%), in accordance with the increased voltage and current demand from the PAL load. Each buck converter circuit monitors the output current through the switching element, via a current sense transformer, for both regulation and maximum current limit considerations. The current limit is ~15 amps for the PAL circuit and ~10 amps for the bore light circuit. Each PWM circuit runs at ~35kHz. RF filtering, in the form of toroidal choke inductors, reside on the rear interface board.

The dock (docking) and long (longitudinal) motor supplies share a common transformer secondary, wherein the 243V is stepped down to ~50V. The 50V is rectified, filtered, and passed on to both the dock and long circuits. A center-tap on the step-down transformer defines a reference for the dock and long PWM IC circuits. The potential of this reference is at ~25V with reference to the return path for the dock motor supply.

4-3 Dock/Light Board (continued)

The dock motor supply is another buck-mode topology converter controlled by a current mode PWM IC. The PWM IC is powered by tapping off the 50Vdc bus, with respect to the 25V reference level, through a current limiting resistor. This PWM IC is enabled by an active low control signal optically coupled from the CPD board. The dock supply consists of the PWM IC and supporting circuitry, a transformer coupled drive circuit, current limit control and feedback circuitry, adjustable output voltage feedback circuit, and a remote sense feedback circuit.

Output voltage control is achieved by a pot, allowing an output voltage swing from ~20 to 40Vdc. The level of output voltage is adjusted proportional to the speed at which the docking motor will raise the table. The PWM IC is run near its maximum duty cycle in order to maintain a nominal 38.5V output voltage. A remote sense amplifier circuit compensates for IR line loss, with more compensation available for lower output voltages.

A transformer-coupled drive circuit for the main switching transistor (similar to the input buck converter on the buck/H-bridge board) allows for fast turn-on and turn-off times, improving the overall control of the circuit. A dual transformer-coupled current sense circuit is used for PWM control and to accurately determine the output current of the supply. A portion of the current limit circuitry is designed to provide a timed current limit above an average current of ~15 amps. T he purpose of the timed current limit is to allow for increased output current draw during start-up of the motor. The timed current limit activates at ~300 milliseconds after more than ~26 amps is drawn from the supply. Once the time limit is exceeded, the current is reduced to 5 amps until the output current is reduced below this 5 amp current limit. The upper limit of current draw by the supply is controlled by the PWM IC and is ~30 amps.

The long drive circuit also monitors the output current level of the dock supply, resulting in the disabling of the long drive PWM IC, as well as a complete disconnect of its output if any significant current draw by the dock supply is achieved. This prevents the possibility of both motors operating at the same time. The dock PWM IC runs at a frequency of approximately 25kHz, and at maximum duty cycles in excess of 90%.

The long drive circuit consists of an H-bridge switch mode converter topology utilizing a dc motor drive controller IC. The H-bridge supply rail is the same 50 volts used by the dock motor supply. The controller IC is powered by linear regulators on both rails of the 50Vdc bus, providing a ±15V supply level to the IC (referenced to the previously described 25V level). The long drive circuitry consists of the motor drive controller IC and its associated control circuitry, the H-bridge drive circuit and switching transistors, the motor command input buffer, an IR compensation feedback circuit, and various enable/disable circuits.

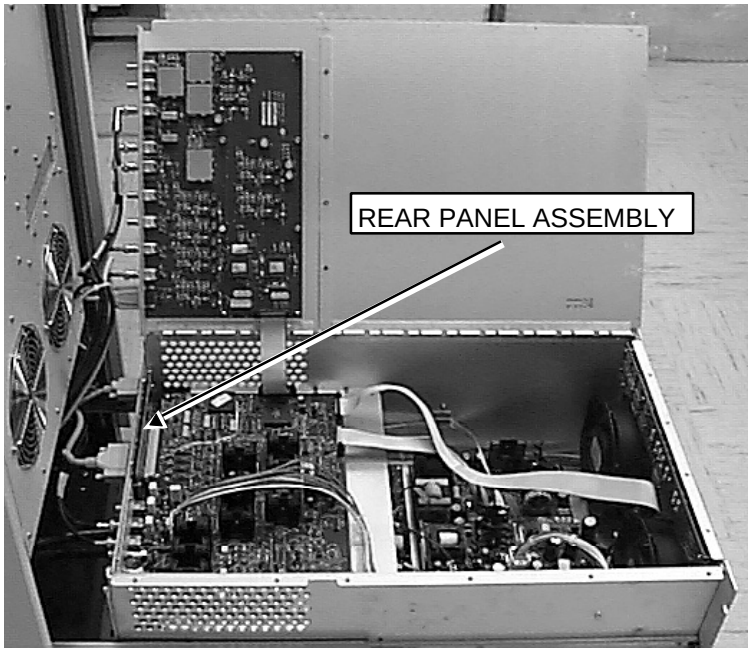
4-3 Dock/Light Board (continued)

Much of the supporting circuitry around the controller IC helps to determine the regulation scheme applied to the output H-bridge. In this case, when the circuit is presented with a zero value motor command, both lower transistors will be on. When a non-zero motor command is input, one of the lower transistors will remain on (depending on the polarity of the motor command), and the other lower transistor will start turning off, while the upper transistor on that same leg starts to turn on. The greater the magnitude of the motor command, the more the upper transistor is left on. Output current is sensed via a sense resistor, and the voltage developed across the sense resistor controls a feedback amplifier circuit that tries to increase the speed of the motor as the output current is increased. This occurs in an attempt to offset the IR loss in the motor and output lines and the resulting decreased motor speed associated with higher output currents. A second unipolar current sense resistor exists in series with the bottom drive transistors on the H-bridge. When the current out of the H-bridge exceeds 5 amps, the voltage developed across this sense resistor will cause a limit of the controller IC. The enable for the long motor supply is an optically-coupled differential signal from the rear interface board. This enable signal serves two functions: enable/disable the motor drive controller IC, and enable/disable a relay in series with one of the output lines. The PWM will also be disabled if either of the 50V supply rails are less than ±18V with respect to the center-tapped reference. Additionally, there is the current sense of the dock supply described earlier, which can inhibit operation of the controller IC. T he controller IC operates at a frequency of ~20kHz.

There is no RF filtering on either the dock motor or long drive output lines. Instead, the PWM ICs are completely disabled during any scanning procedure.

5- REAR PANEL ASSEMBLY

The rear panel assembly is the power distribution portion of the SSM. It distributes the incoming ac voltage as well as all of the output supplies, both ac and dc. See Illustration 5-1 and Illustration 1-11.



REAR PANEL ASSEMBLY LOCATION
ILLUSTRATION 5-1

The three-phase input power from the 208VAC five-pin connector is tied to CB4 (the main breaker). A jumper wire is attached on each phase and is distributed to the following locations:

Phase A goes to CB1 and one phase of the amplifiers.
Phase B goes to CB2 and one phase of the amplifiers.
Phase C goes to CB3 and the final phase of the Erbtec amplifier power.

CB4 delivers power to the internal power supply for the module. CB1 controls the power to the bore vent. (The voltage is actually switched through a solid state relay on the power supply.) CB2 controls the gradient fan, and CB3 controls the service duplex outlet on the front panel of the SSM.

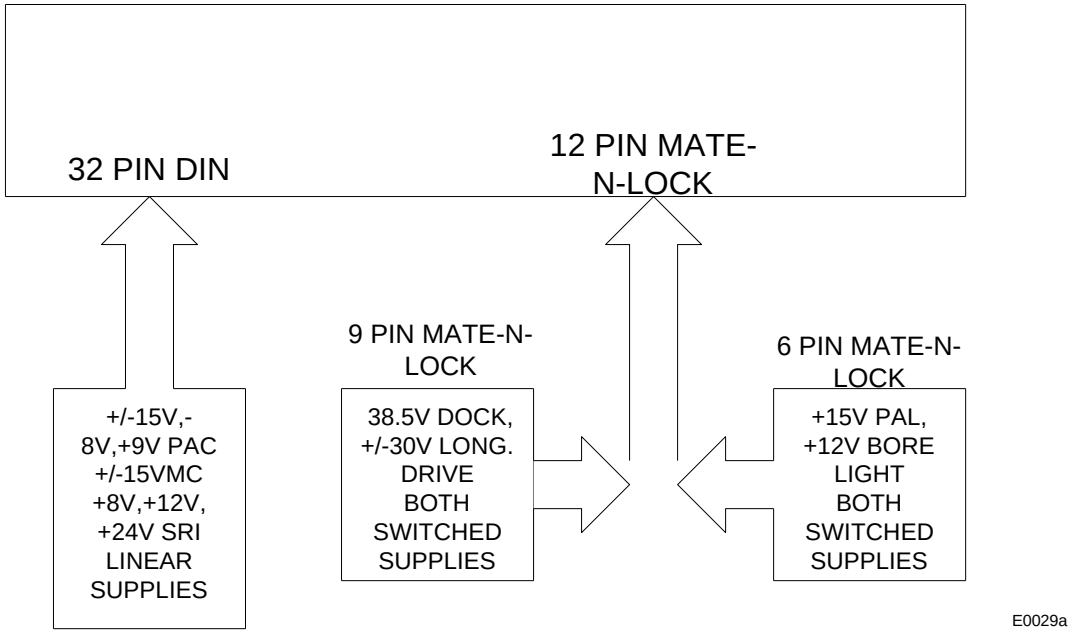
CAUTION

Possible personal injury. The amplifier power cords are live whenever power is connected to the unit.

The 120VAC for both the gradient fan and bore vent are supplied via three phase Phoenix connectors, the center pin being ground. As stated above, both are controlled by a circuit breaker.

5- REAR PANEL ASSEMBLY (continued)

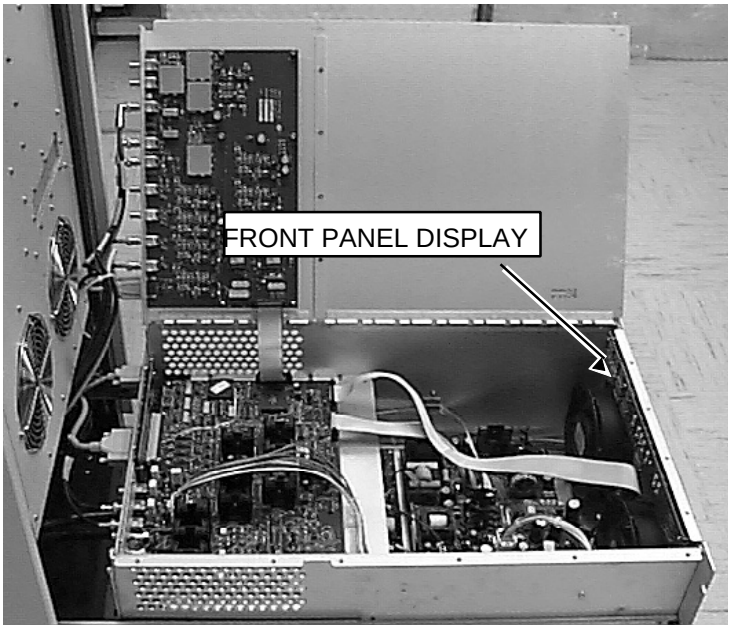
All dc supplies are routed through the rear panel, specifically through the rear interface board. The switched supplies come onto the board via one 6-pin and one 9-pin connector from the dock/light board combining into one 12-pin connector on the rear interface board. The linear supplies are brought onto the board via a 32-pin connector coming from the buck/H-bridge board. See Illustration 5-2.



REAR INTERFACE BOARD CONNECTIONS
ILLUSTRATION 5-2

6- FRONT PANEL DISPLAY BOARD

See Illustration 6-1. The front panel display provides the necessary controls and displays to perform all standard servicing (field adjustments, periodic checks, and diagnostics) without opening the lid, except for the TR, Multi-coil, and power supplies. With one exception (the HV enable switch), all LEDs and switches are directly decoded by the microprocessor, which then executes the command, or displays the requested information.



FRONT PANEL DISPLAY LOCATION
ILLUSTRATION 6-1

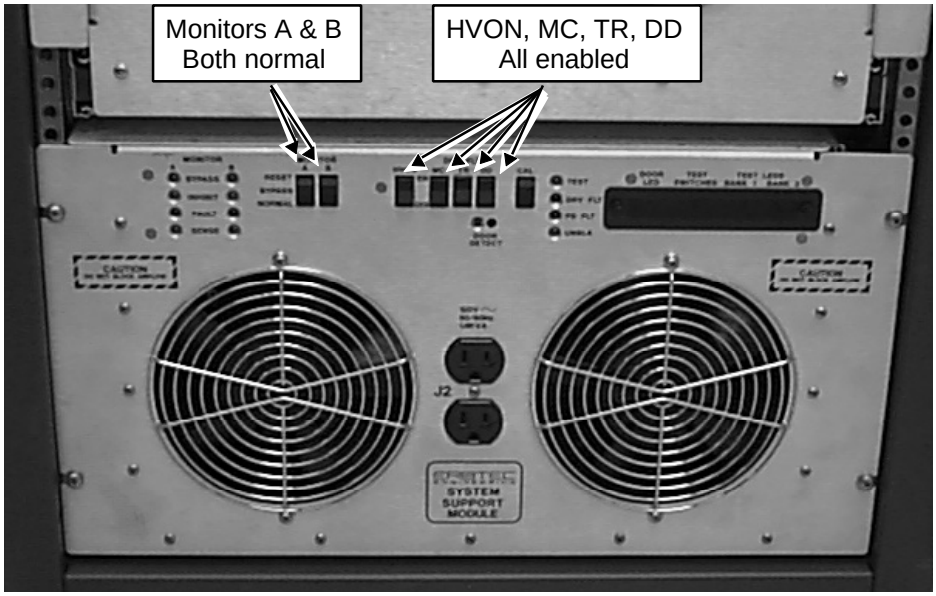
Consequently, all interactions that are possible using the front panel display are also possible using the auxiliary RS-232 port and, in many cases, are possible using the MDS optical link. Laptop computer software has been provided which uses the RS-232 port and assists in these interactions. Go to the *Laptop Troubleshooting Software Diagnostic Procedure* for directions using the software.

The front panel display consists of a collection of switches and LEDs. The switches from left to right are:

- Monitor A reset/bypass/normal
- Monitor B reset/bypass/normal
- HVON enable/disable
- MC fault enable/disable
- TR fault enable/disable
- DD fault enable/disable
- CAL (DD open circuit fault calibrate)

6- FRONT PANEL DISPLAY BOARD (continued)

The "normal operation" position of all switches is shown in Illustration 6-2.



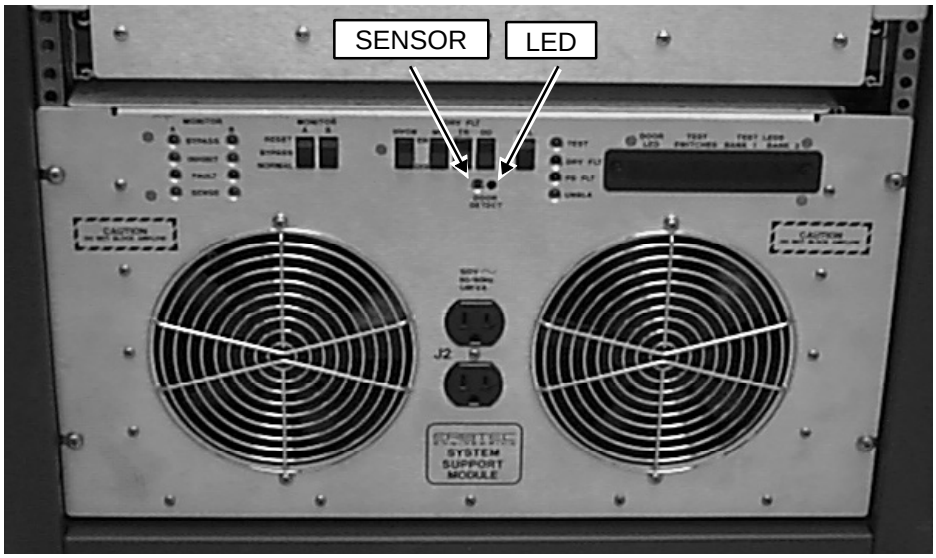
FRONT PANEL SWITCHEDDS IN NORMAL POSITION
ILLUSTRATION 6-2

The LEDs from left to right are:

Monitor A (status) BYPASS, INHIBIT, FAULT, SENSE
Monitor B (status) BYPASS, INHIBIT, FAULT, SENSE
(general fault status) TEST, DRV FLT, PS FLT, UNBLNK
DOOR LED (concealed behind the test window)

6- FRONT PANEL DISPLAY BOARD (continued)

The front door is detected by pulsing power through an IR LED while looking for a correlated reflection off the door at a nearby IR sensor. Physical locations are shown in Illustration 6-3. The door is presumed to be present whenever the IR detector sees a signal that correlates to the pulsing IR LED. An amber-colored LED located behind the test window indicates the door status. LED lit indicates door off. The IR LED is pulsed at ~150Hz.



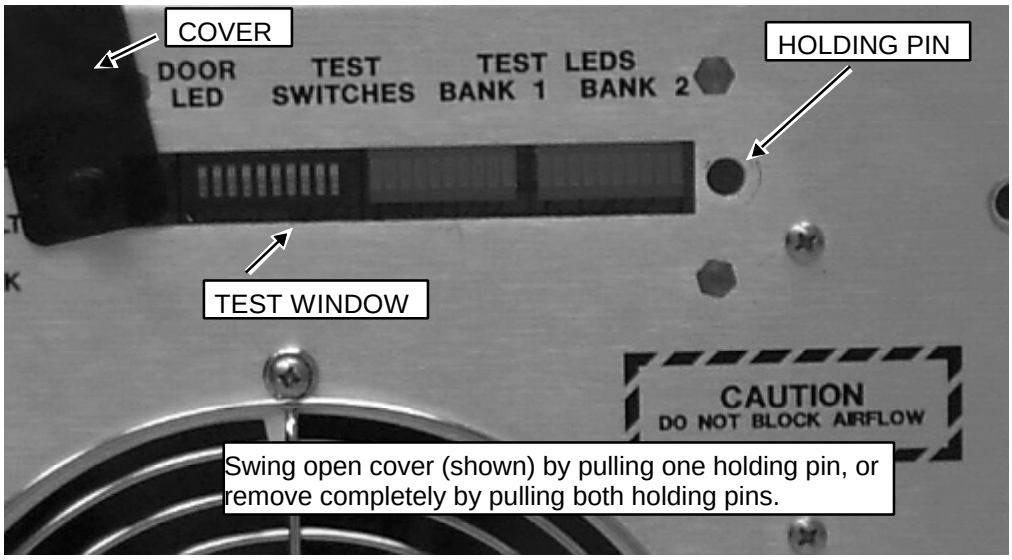
IR SENSOR AND LED LOCATIONS
ILLUSTRATION 6-3

Software on the CPD prevents the safety monitors from being bypassed while the front door is off. If objects (such as a wall, a cardboard box, or even a technician) are positioned immediately in front of the front panel, the safety monitors may enable themselves. Service personnel can observe the effects of this detector by placing the monitors in bypass (LED should light). Then move an object (box, book, hand, etc.) in front of the detector and watch the bypass LED change to normal (off).

6-1 Test Window

The right side of the front panel contains a removable transparent plastic cover. It can be removed by pulling the two holding pins at the outer edges. Underneath the cover are a single LED, 10 switches (in a DIP package) and 20 LEDs (in 2 DIP packages); see Illustration 6-4. These switches and LEDs provide the service personnel with the ability to implement all standard service procedures without the use of an external laptop computer. However, the use of a laptop computer, if available, is generally preferable as it provides more capabilities.

6-1 Test Window (continued)



REMOVABLE TEST WINDOW COVER
ILLUSTRATION 6-4

6-1 Test Window (continued)

See Table 6-1. Spectro refers to the Multi-Nuclear Spectroscopy (MNS) option (not available with 0.7T).

TABLE 6-1
TEST SWITCH AND TEST LED DEFINITIONS

Task	Switch Number	Position	Item Controlled	LED Bank 1	LED Bank 2
Normal Operation:	1	Down		MDS comm status	Head T/R fault
	2	--------	(When one	NB comm status	Body T/R fault
	3	--------	of these 10 is	Monitor A comm status	Spectro T/R fault
	4	--------	in use,	Monitor B comm status	Body Coil 1 fault
	5	--------	the others	PS fault	Dyn Disable fault
	6	--------	are inactive)	top cover open	Body Coil 2 fault
	7	--------		MC faults disabled	Multicoil 1 fault
	8	--------		T/R faults disabled	Multicoil 2 fault
	9	--------		DD faults disabled	Multicoil 3 fault
	10	--------		DD open ckt adj failure	Multicoil 4 fault
Static Control of Drivers:	1	UP		Head TR open	Dyn Disable open
	2	DOWN		Head TR short	Dyn Disable short
	3	DOWN		Body TR open	Multicoil 1 short
	4	DOWN		Body TR short	Multicoil 1 open
	5	UP	MC1 drv enable	Spectro TR open	Multicoil 2 short
	5	DOWN	MC1 drv disable		
	6	UP	MC2 drv enable	Spectro TR short	Multicoil 2 open
	6	DOWN	MC2 drv disable		
T/Rs Disabled:	7	UP	MC3 drv enable	Body Coil 1 open	Multicoil 3 short
	7	DOWN	MC3 drv disable		
	8	UP	MC4 drv enable	Body Coil 1 short	Multicoil 3 open
	8	DOWN	MC4 drv disable		
	9	UP	Source Mode	Body Coil 2 open	Multicoil 4 short
	10	UP			
	9	DOWN	Sink Mode	Body Coil 2 short	Multicoil 4 open
	10	DOWN			
Pulse Control of Drivers:	1	UP		Head TR open	Dyn Disable open
	2	DOWN		Head TR short	Dyn Disable short
	3	DOWN		Body TR open	Multicoil 1 short
	4	DOWN		Body TR short	Multicoil 1 open
	5	UP	MC1 drv enable	Spectro TR open	Multicoil 2 short
	5	DOWN	MC1 drv disable		
	6	UP	MC2 drv enable	Spectro TR short	Multicoil 2 open
	6	DOWN	MC2 drv disable		
	7	UP	MC3 drv enable	Body Coil 1 open	Multicoil 3 short
	7	DOWN	MC3 drv disable		
	8	UP	MC4 drv enable	Body Coil 1 short	Multicoil 3 open
	8	DOWN	MC4 drv disable		
	9	UP	Source Mode	Body Coil 2 open	Multicoil 4 short
	10	UP			
	9	DOWN	Sink Mode	Body Coil 2 short	Multicoil 4 open
	10	DOWN			

Task	Switch Number	Position	Item Controlled	LED Bank 1	LED Bank 2
PS Override Tests	1	UP		Head TR open	Dyn Disable open
	2	DOWN		Head TR short	Dyn Disable short
	3	UP		Body TR open	Multicoil 1 short
	4	DOWN		Body TR short	Multicoil 1 open
	5	UP	MC1 drv enable	Spectro TR open	Multicoil 2 short
	5	DOWN	MC1 drv disable		
	6	UP	MC2 drv enable	Spectro TR short	Multicoil 2 open
	6	DOWN	MC2 drv disable		
	7	UP	MC3 drv enable	Body Coil 1 open	Multicoil 3 short
	7	DOWN	MC3 drv disable		
	8	UP	MC4 drv enable	Body Coil 1 short	Multicoil 3 open
	8	DOWN	MC4 drv disable		
	9	UP	Source Mode	Body Coil 2 open	Multicoil 4 short
	10	UP			
	9	DOWN	Sink Mode	Body Coil 2 short	Multicoil 4 open
	10	DOWN			
PS Override Tests	1	UP		Dock enable	--------
	2	DOWN		PAC 8V	--------
	3	DOWN		PAC 9V	–5V Supply too high
	4	UP			–15V Supply too high
	5	UP	Dock disable	Bore vent	+15V Supply too high
	5	DOWN	Dock enable		
	6	UP	PAC 9V	Patient Alignment light	HV Sense too high
	6	DOWN	PAC 8V		
	7	UP	Bore light enable	Bore light	–5V Supply too low
	7	DOWN	Bore light disable		
	8	UP	PAL enable	--------	–15V Supply too low
	8	DOWN	PAL disable		
	9	UP	Bore vent enable	MCD enable	+15V Supply too low
	9	DOWN	Bore vent disable		
	10	--------		--------	HV sense too low
				Monitor A	Monitor B
Monitor Fault Summary	1	UP		RF without unblank	RF without unblank
	2	UP		–15V Supply fault	–15V supply fault
	3	DOWN		Body Pwr limit fault	Body pwr limit fault
	4	UP		Head Pwr limit fault	Head pwr limit fault
	5	--------		Spectro Pwr limit fault (Multi-Nuclear)	Spectro pwr limit fault
	6	--------		Duty Cycle fault	Duty cycle fault
	7	--------		RF Pulse Width fault	RF pulse width fault
	8	--------		+15V Supply fault	+15V supply fault
	9	--------		Body Cable fault	Body cable fault
	10	--------		Head/Spectro Cable fault	Head/Spectro cable fault
Multicoil Configuration	1	UP		Multicoil 1 enable	--------
	2	DOWN		Multicoil 2 enable	--------

Task	Switch Number	Position	Item Controlled	LED Bank 1	LED Bank 2
Multicoil Configuration	3	UP		Multicoil 3 enable	--------
(continued)	4	UP		Multicoil 4 enable	--------
	5	UP	MC1 enable	--------	--------
	5	DOWN	MC1 disable		
	6	UP	MC2 enable	--------	--------
	6	DOWN	MC2 disable		
	7	UP	MC3 enable	--------	--------
	7	DOWN	MC3 disable		
	8	UP	MC4 enable	--------	--------
	8	DOWN	MC4 disable		
	9	--------		--------	--------
	10	UP, then DOWN	Program	--------	--------
Monitor Type Configuration	1	UP		--------	--------
	2	UP		Monitor A 1.0T	Monitor B 1.0T
	3	UP		--------	--------
	4	UP		Monitor A 1.5T w/EFB	Monitor A 1.5T w/EFB
	5	UP, 6 DOWN=1.0T		--------	--------
	5	UP AND 6 UP=1.5T		--------	--------
	7	--------		--------	--------
	8	--------		--------	--------
	9	--------		--------	--------
	10	UP, then DOWN	Program	--------	--------

7- LAPTOP SOFTWARE

Two DOS-executable programs have been provided to assist in servicing the cabinet. They are MONS.EXE and CPD.EXE. Use of these files are covered in the *Laptop Troubleshooting Software Diagnostic Procedure*.

REVISION HISTORY

REV	DATE	AUTHOR	PRIMARY REASONS FOR CHANGE
A	December 7, 1999	Resa Lambert	Preliminary version.
0			Initial Release.