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**Note**

Calibration with Spectro Option - For a Signa 1.5T system with the spectroscopy option, refer to Direction 2151387, Signa Horizon Spectroscopy Subsystem, Set Up and Calibration tab, Section 1, Broadband and Narrow Band RF Cabinets for Broadband RF Amplifier output calibration.

**Description -** The 1.5T PIN Switch Driver Board of the RF System Controller (RFSC) module provides the dc bias signals needed for switching the various transmit/receive (TR) switches, dynamic disable switches, and direct drive switches.

**Note**

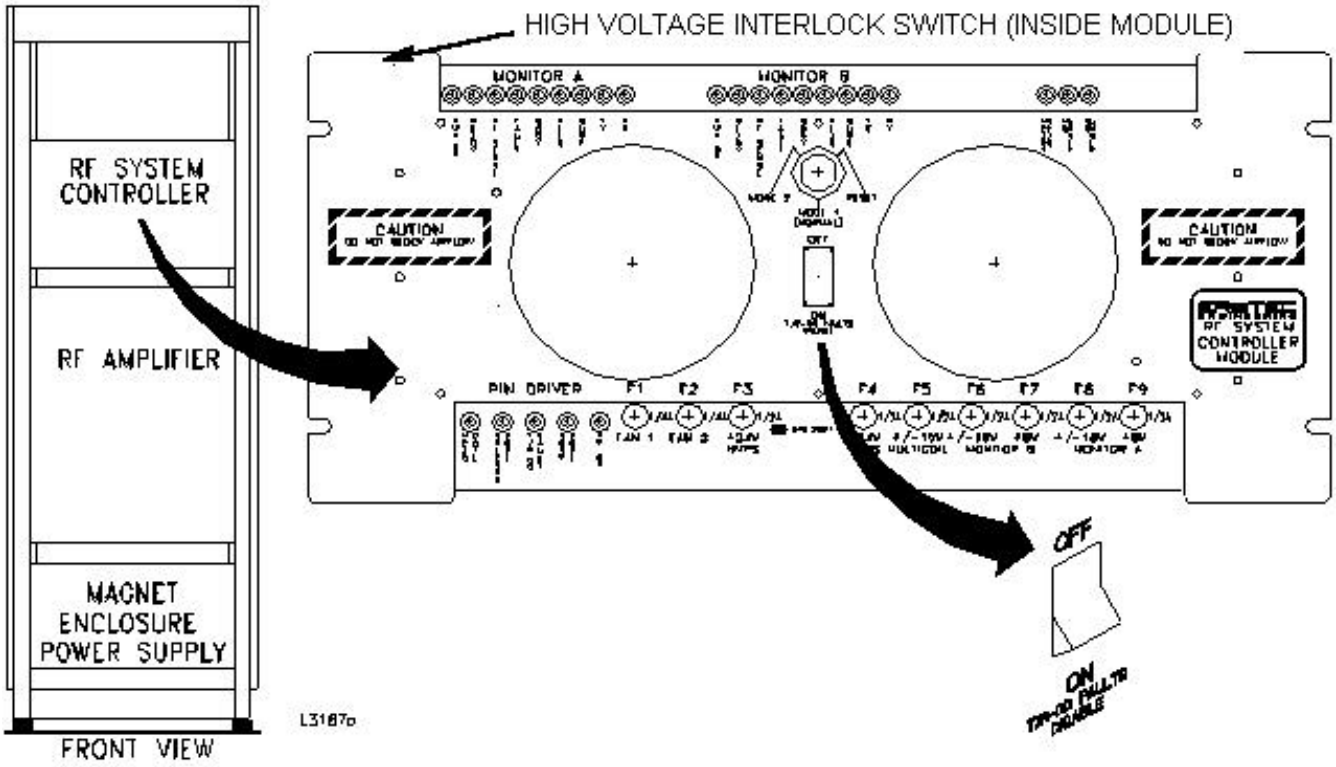
This procedure is to be used for systems that contain an RF/PEN Cabinet (5.5 and later). See procedure for Dynamic Disable / TR Driver board adjustment for systems with both **RF and Penetration** cabinets (5.4 and prior). See procedure for Communications Pin Driver set up and calibration for **RF/PEN II** cabinets.

**NOTE**

Non- Multicoil systems make sure to read Section 4- Multicoil Driver Circuit Adjustments step # 9.

**WARNING!**

**POSSIBLE ELECTRIC SHOCK! USE EXTREME CARE WHEN REMOVING OR REPLACING JUMPERS IN THE MODULE. THERE IS 1000 VDC AND 120 VAC PRESENT INSIDE THE MODULE. USE THE HV INTERLOCK TO SHUT OFF HIGH VOLTAGE. VERIFY THE *HV O*N LED IS OFF (SEE ILLUSTRATION L3167A).**




**DYNAMIC DISABLER / TR DRIVER IN NORMAL POSITION**
ILLUSTRATION L3167A

Record all measurements performed in the procedure for future reference as a troubleshooting aid. Refer to Table 13 to record the measurements.

TABLE 13
**PIN SWITCH DRIVER BOARD CALIBRATION DATA**

| Step | Function | Location | Pot. Adj. | Meas. Value | Specification |
|---|---|---|---|---|---|
| 2-8 | –15 V_A Power Supply | TP56 (W/ TP58) | | | |
| 2-8 | +15 V_A Power Supply | TP51 (W/ TP58) | | | |
| 2-8 | +5 Vdc Power Supply | TP54 (W/ TP58) | | | +5.0 ± 0.25 Vdc |
| 2-8 | –15 Vdc Power Supply | TP57 (W/ TP58) | | | –15.0 ± 0.2 Vdc |
| 2-8 | +15 Vdc Power Supply | TP55 (W/ TP58) | | | +15.0 ± 0.2 Vdc |
| 2-8 | +500/1000 Vdc Power Supply | TP62 (W/ TP58) | | | +500 ± 25 Vdc<br>+1000 ± 50 Vdc |
| 3-3a | Direct Drive Output (J402 Connected) | TP40 (W/TP56) | | | 1.1 ± 0.2 Vdc |
| 3-4a | Dyn. Dis. Driver #1 (J403 Connected) | TP32 (W/TP56) | | | +1.0 ± 0.2 Vdc |
| 3-5a | Dyn. Dis. Driver #2 (J401 Connected) | TP46 (W/TP56) | | | +1.0 ± 0.2 Vdc |
| 3-6 | Direct Drive Output Voltage | TP38 (W/TP59) | | | –2.5 ± 1.0 Vdc (FIXED) |
| 3-7a | Dyn. Dis. Driver #1 (Loaded) | TP31 (W/TP59) | | | –5.0 ± 1.5 Vdc (FIXED) |
| 3-7b | Dyn. Dis. Driver #2 (Loaded) | TP46 (W/TP59) | | | –5.0 ± 1.5 Vdc (FIXED) |
| 3-8 | Direct Drive Open Circuit Detect | TP44 (W/TP59) | R207 | | Value @ TP45 –3.0 ± 0.1 Vdc (Rev. B Body Hybrid) |
| | | | | | Value @ TP45 –2.0 ± 0.1 Vdc (Normal) |
| 3-8 | Dyn. Dis. Driver #1 Open Cir. Detect | TP34 (W/ TP59) | R147 | | Value @ TP33–3.0 ± 0.1 Vdc<br><br>(Rev. B Body Hybrid)<br>Value @ TP33 –2.0 ± 0.1 Vdc (Normal) |
| 3-8 | Dyn. Dis. Driver #2 Open Cir. Detect | TP48 (W/ TP59) | R228 | | Value @ TP47 –3.0 ± 0.1 Vdc<br><br>(Rev. B Body Hybrid)<br>Value @ TP47 –2.0 ± 0.1 Vdc (Normal) |
| 3-11 | Direct Drive Output Voltage | TP38 (W/TP59) | | | Value @ TP62+0/–10 Vdc |
| 3-12b | Dyn. Dis. Driver #2 Output Voltage | TP46 (W/TP59) | | | Value @ TP62 +0/–10.0 Vdc |
| 4-3b | TR Driver (Body) (Loaded) | TP16 (W/TP59) | R13 | | +4.0 ± 0.1 Vdc |
| 4-3d | TR Driver (Head) (Loaded) | TP9 (W/TP59) | R26 | | +8.0 ± 0.1 Vdc |
| 4-3f | TR Driver (Spectro) (Loaded) | TP21 (W/TP59) | R18 | | +4.0 ± 0.1 Vdc |
| 4-4a | TR Driver (Body) (Loaded) | TP13 (W/TP59) | | | > Value @ TP12 |
| 4-4b | TR Driver (Head) (Loaded) | TP1 (W/TP59) | | | > Value @ TP17 |
| 4-4c | TR Driver (Spectro) (Loaded) | TP18 (W/TP59) | | | > Value @ TP19 |
| 4-7 | Head TR Current Output | TP1 (W/TP59) | | | 0.0 ± 0.1 Vdc |
| 4-7 | Head TR Voltage Output | TP9 (W/TP59) | | | –13.75 ± 1.5 Vdc |
| 4-7 | Body TR Current Output | TP13 (W/TP59) | | | 0.0 ± 0.25 Vdc |
| 4-7 | Body TR Voltage Output | TP16 (W/TP59) | | | –13.75 ± 1.5 Vdc |
| 4-7 | Spectro TR Current Output | TP18 (W/TP59) | | | 0.0 ± 0.25 Vdc |

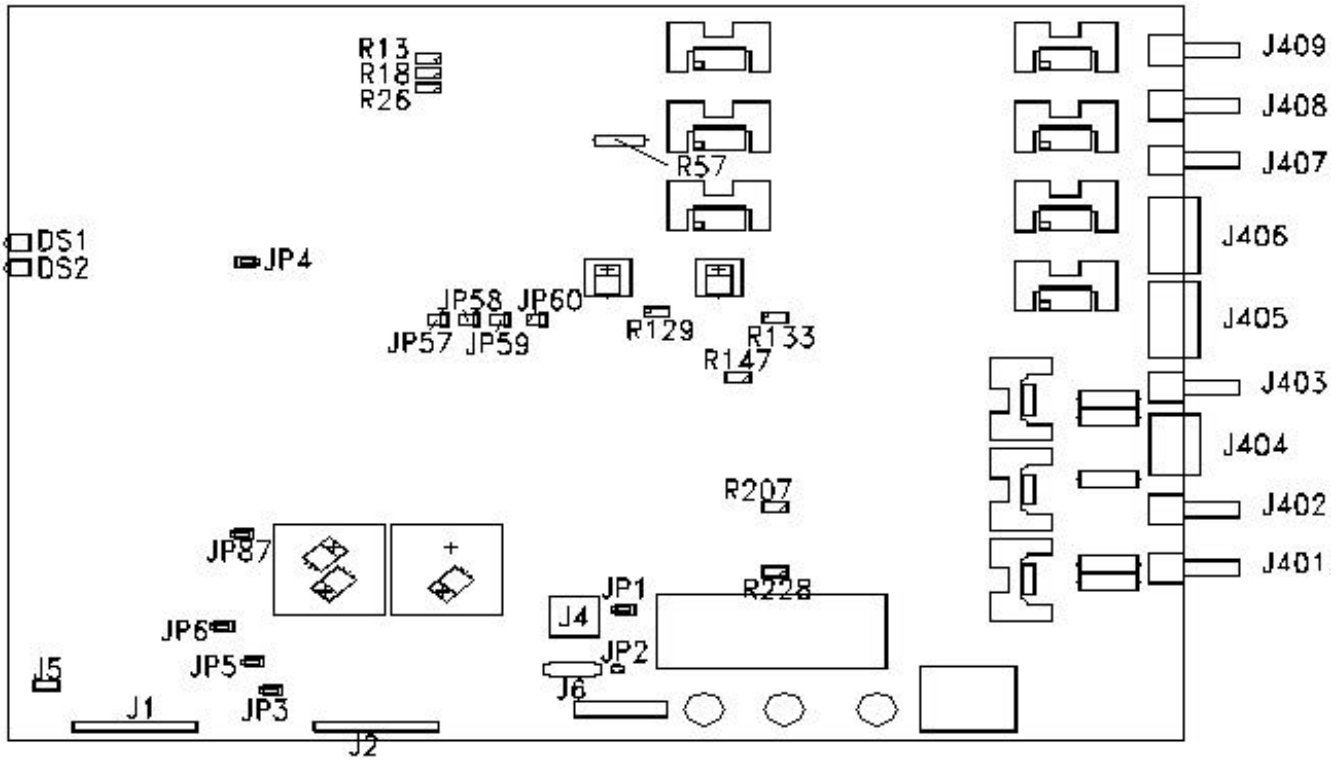
| | | | | | |
|---|---|---|---|---|---|
| 4-7 | Spectro TR Voltage Output | TP21 (W/TP59) | | | –13.75 ± 1.5 Vdc |
| 4-9e | TR Driver Circuit | TP16 | R13 | | +4.0 ± 0.5 Vdc |
| 4-9e | TR Driver Circuit | TP9 | R26 | | +8.0 ± 0.5 Vdc |
| 4-9e | TR Driver Circuit | TP21 | R18 | | +4.0 ± 0.5 Vdc |
| 5-3b | Multicoil 1 (Loaded) (Transmit) | TP2 (W/TP59) | R133 | | +5.0 ± 0.1 Vdc |
| 5-3c | Multicoil 2 (Loaded) (Transmit) | TP14 (W/TP59) | | | +5.0 ± 0.1 Vdc |
| 5-3c | Multicoil 3 (Loaded) (Transmit) | TP20 (W/TP59) | | | +5.0 ± 0.1 Vdc |
| 5-3c | Multicoil 4 (Loaded) (Transmit) | TP26 (W/TP59) | | | +5.0 ± 0.1 Vdc |
| 5-5b | Multicoil 1 (Loaded) (Receive) | TP2 (W/TP59) | R129 | | –5.0 ± 0.1 Vdc |
| 5-5c | Multicoil 2 (Loaded) (Receive) | TP14 (W/TP59) | | | –5.0 ± 0.1 Vdc |
| 5-5c | Multicoil 3 (Loaded) (Receive) | TP20 (W/TP59) | | | –5.0 ± 0.1 Vdc |
| 5-5c | Multicoil 4 (Loaded) (Receive) | TP26 (W/TP59) | | | –5.0 ± 0.1 Vdc |
| 5-6b | Multicoil 1 Error Detect | TP7 (W/TP59) | | | <TP8 (Loaded) (Transmit) |
| 5-6c | Multicoil 2 Error Detect | TP11 (W/TP59) | | | <TP3 (Loaded) (Transmit) |
| 5-6d | Multicoil 3 Error Detect | TP22 (W/TP59) | | | <TP25 (Loaded) (Transmit) |
| 5-6e | Multicoil 4 Error Detect | TP28 (W/TP59) | | | <TP24 (Loaded) (Transmit) |
| 5-7a | Multicoil 1 Error Detect | TP7 (W/TP59) | | | <TP10 and >TP8 (Loaded) (Receive) |
| 5-7b | Multicoil 2 Error Detect | TP11 (W/TP59) | | | <TP4 and >TP3 (Loaded) (Receive) |
| 5-7c | Multicoil 3 Error Detect | TP22 (W/TP59) | | | <TP23 and >TP25 (Loaded) (Receive) |
| 5-7d | Multicoil 4 Error Detect | TP28 (W/TP59) | | | <TP27 and >TP24 (Loaded) (Receive) |

## 1- PIN SWITCH DRIVER BOARD INITIAL SETUP

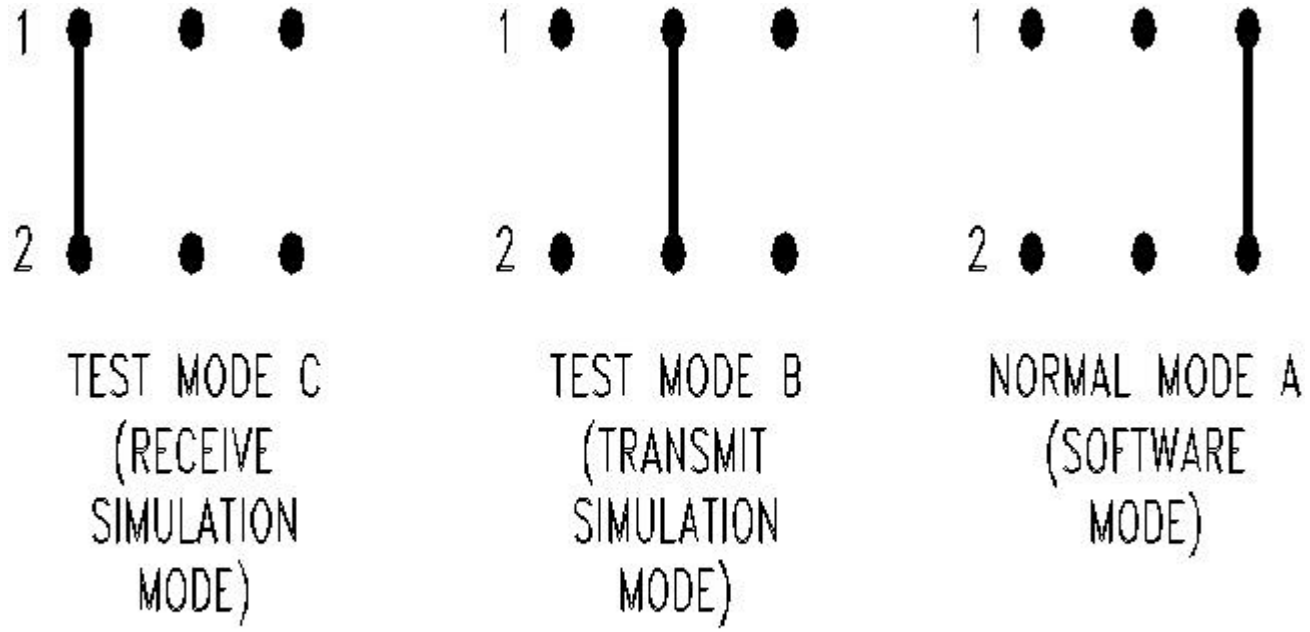
1. Remove the rear shield from the top of the RFSC module to obtain access to some of the test points.

2. Verify that T/R-DD Faults Disable switch is off (faults not disabled) on the RFSC module (MR1A15). See Illustration L3167a before section 1.

3. Verify that jumpers JP57–60 are in software control mode (normal mode, pins 5 and 6 connected) for four-channel multicoil systems, or in b mode (receive mode, pins 3 and 4 connected) for nonmulticoil systems. For two-channel multicoil systems, verify that JP57 and JP59 are in software control mode (normal mode, pins 5 and 6 connected), and that JP58 and JP60 are in b mode (receive mode, pins 3 and 4 connected). See Illustration L3133a and Illustration L3169b.

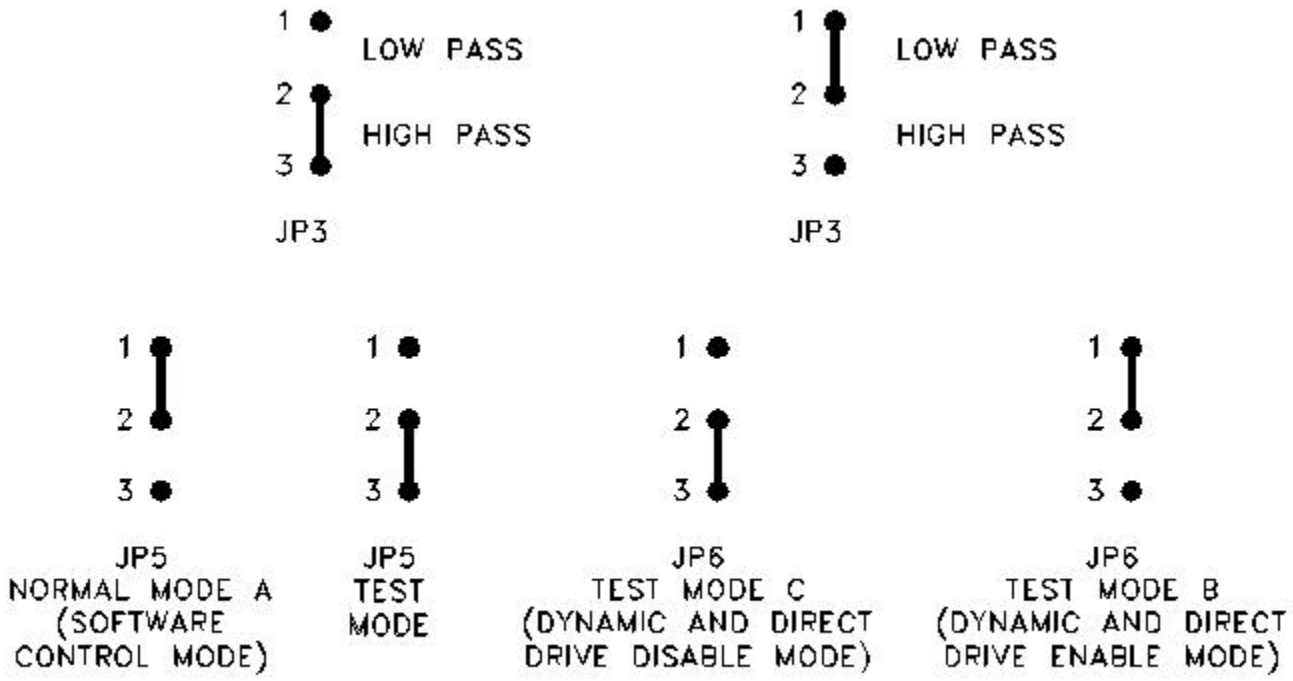



**PIN SWITCH DRIVER BOARD LAYOUT / JUMPERS**
ILLUSTRATION L3133A

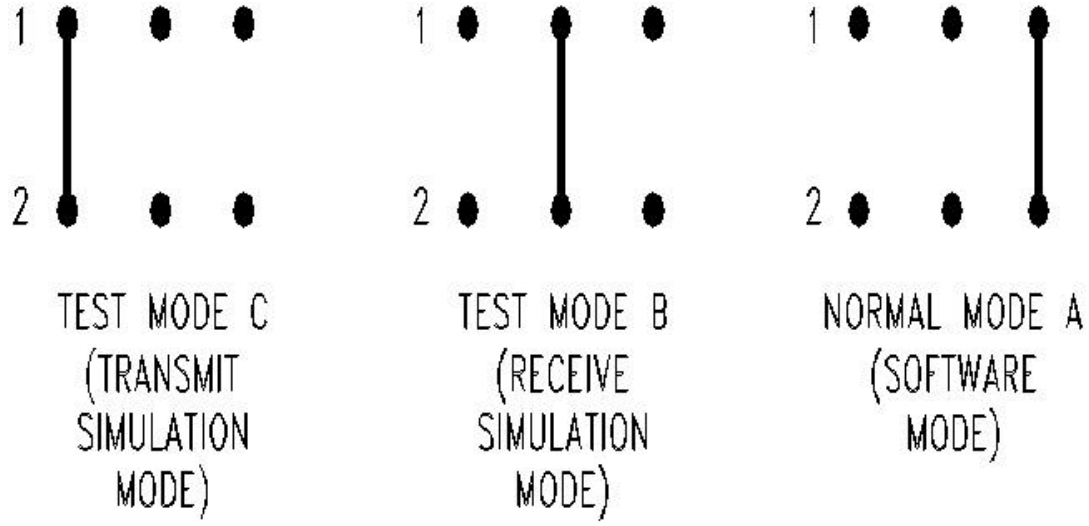



**JUMPER JP57–JP60 MODE POSITIONS**
ILLUSTRATION L3169B

4. Verify that jumper JP87 is in software control mode (normal mode, pins 5 and 6 connected). Verify that JP5 is in normal mode, (pins 1 and 2 connected). See Illustration L3133a and Illustration L3169a and Illustration L3168a.




**JUMPER JP5, JP6, AND JP3 MODE POSITIONS**
ILLUSTRATION L3168A




**JUMPER JP87 MODE POSITIONS**
ILLUSTRATION L3169A

5. Verify that jumper JP3 is in high pass mode. See Illustration L3133a and Illustration L3168a above.

6. Verify that jumper JP1 is in 1000V mode for 1.5T systems, or in 500V mode for 1.0T systems. See Illustration L3133a above.

7. Place JP5 across pins 2 and 3 (test mode), and JP6 across pins 1 and 2 (dynamic and direct drive enable, test mode "B") on PIN Switch Driver Board. See Illustration L3133a and Illustration L3168a above.

**Note**

Check Body Coil LED - The Body Coil LED on the front panel of the RFSC module should be lit. This sets a positive output voltage for the dynamic and direct drive disable circuits, which simulate the operation of the circuits during body mode.

8. Measure and verify the outputs of test points on PIN Switch Driver Board. Refer to Table 1 and Illustration L3133b above. Verify that the High Voltage Interlock switch is pulled up to enable the high voltage on the PIN Switch Driver Board. Refer to Illustration L3167a before Section 1.

**Note**

Measurements Should Be Made In Reference To LGND - Although the Dynamic Disable module is grounded to the chassis, all measurements should be made in reference to LGND (TP58, logic ground) on the board, and not to the module chassis, unless otherwise stated. Incorrect measurement readings could occur if chassis is used as the reference.

## 2- DIRECT DRIVE & BODY COIL DISABLE OPEN CIRCUIT THRESHOLD ADJUSTMENTS

1. Verify that T/R-DD faults disable switch is off (faults not disabled) on the RFSC module. See Illustration L3167a before Section 1.

2. Move JP5 and JP6 across pins 2 and 3 (test mode and test mode "C"). See Illustration L3133a and Illustration L3168a in Section 1. Ensure that jumper JP3 is across pins 2 and 3 (high pass mode).

**Note**

Body Coil LED - The Body Coil LED at the front of the RFSC module should be off. This sets a negative output voltage for the direct drive disable circuit that simulates the operation of this circuit during head mode.

3. Check the Direct Drive and Body Coil Output Current on the PIN Switch Driver Board as follows: Refer to Table 2.

TABLE 2
**DIRECT DRIVE AND DYNAMIC DISABLE DRIVER (LOADED) CALIBRATION DATA**

| Step | Function | Location | Pot. Adj. | Specification |
|---|---|---|---|---|
| 3-3a | Direct Drive (J402 Connected) | TP40 (W/ TP56) | None | +1.1 ±0.2 Vdc |
| 3-4a | Dyn. Dis. Driver #1 (J403 Connected) | TP32 (W/ TP56) | None | +1.0 ±0.2 Vdc |
| 3-5a | Dyn. Dis. Driver #2 (J401 Connected) | TP49 (W/ TP56) | None | +1.0 ±0.2 Vdc |

a. Measure the voltage at TP40 with respect to –15V_A (TP56). It should be 1.0 ± 0.2Vdc. The output current is equal to this voltage.

4. Check Dynamic Disable Driver #1 (Body Coil #1) output current on PIN Switch Driver Board as follows: Refer to Table 2 above.

   a. The voltage at TP32 with respect to -15V_A (TP56) should be 1.0 ±0.2 Vdc. The output current is equal to twice this voltage.

5. Check Dynamic Disable Driver #2 (Body Coil #2) output current on PIN Switch Driver Board as follows: Refer to Table 2 above.

   a. The voltage at TP49 with respect to –15V_A (TP56) should be 1.0 ±0.2 Vdc. The output current is equal to twice this voltage.

6. Measure the loaded output voltage at TP38. Voltage should equal –2.5V ±1.0 Vdc (fixed).

7. Measure the loaded Dynamic Disable Driver voltages on PIN Switch Driver Board as follows: Refer to Table 3.

TABLE 3
**DYNAMIC DISABLE DRIVER CALIBRATION DATA**

| Step | Function | Location (Silk Screen) | Pot. Adj. | Specification |
|---|---|---|---|---|
| 3-7a | Dyn. Dis. Driver 1(Loaded) | TP31 (W/TGND, TP59) | | –5.0 ±1.5 Vdc (FIXED) |
| 3-7b | Dyn. Dis. Driver #2 (Loaded) | TP46 (W/TGND, TP59) | | –5.0 ±1.5 Vdc (FIXED) |

   a. Measure Driver #1 output voltage at TP31 with respect to TGND (TP59). Voltage should equal –5.0 ±1.5 Vdc (fixed).

   b. Measure Driver #2 output voltage at TP46 with respect to TGND (TP59). Voltage should equal –5.0 ±1.5 Vdc (fixed).

**Note**

Driver Output Voltages Vary - The output voltages of the drivers vary from front to back due to differences in the coil loading.

8. Adjust the Direct Drive Open Circuit Detection Level on the PIN Switch Driver Board as shown in Table 4.

TABLE 4
**OPEN CIRCUIT DETECTION CALIBRATION DATA**

| Step | Function | Location (Silk Screen) | Pot. Adj. | Specification |
|---|---|---|---|---|
| 3-8 | DD | TP45 (W/TGND,TP59) | R207 | TP44 = (TP45 -2) ± 0.1 V (Normal)<br>TP44 = (TP45 -3) ± 0.1 V (Rev. B Body Hybrid) |
| | Body 1 | TP33 (W/TGND,TP59) | R147 | TP34 = (TP33 -2) ± 0.01 V (Normal)<br>TP44 = (TP45 -3) ± 0.1 V (Rev. B Body |

| | | | | |
|---|---|---|---|---|
| | | | | Hybrid) |
| | Body 2 | TP47 (W/TGND,TP59) | R228 | TP48 = (TP47 -2) ± 0.01 V (Normal)<br>TP44 = (TP45 -3) ±0.1 V (Rev. B Body Hybrid) |

a. Measure the voltage at TP45 with respect to TGND (TP59).

b. Measure the voltage at TP44 with respect to TGND (TP59). This is the open circuit detection level for this circuit.

c. Adjust R207 until voltage at TP44 is –2 ±0.1 Vdc (Normal), or –3.0 ±0.1 Vdc (Rev. B Body Hybrid) more negative than the measurement taken at TP45.

9. Adjust the Dynamic Disable Driver Open Circuit Detection Levels on PIN Switch Driver Board as shown in Table 4 above.

a. Measure the voltage at TP33 with respect to TGND (TP59).

b. Measure the voltage at TP34 with respect to TGND (TP59). This is the open circuit detection level for Dynamic Disable Driver #1.

c. Adjust R147 until voltage at TP34 is –2 ±0.01 Vdc (Normal), or –3.0 ±0.1 Vdc (Rev. B Body Hybrid) more negative than the measurement taken at TP33.

d. Measure the voltage at TP47 with respect to TGND (TP59).

e. Measure the voltage at TP48 with respect to TGND (TP59). This is the open circuit detection level for Dynamic Disable Driver #2.

f. Adjust R228 until voltage at TP48 is –2 ±0.01 Vdc (Normal), or –3.0 ±0.1 Vdc (Rev. B Body Hybrid) more negative than the measurement taken at TP47.

10. Move jumper JP6 across pins 1 and 2 (Dynamic & Direct Drive Enable, Test Mode "B") on the PIN Switch Driver Board. See Illustration L3133a and Illustration L3168a in Section 1.

**Note**

Body Coil LED Check - The Body Coil LED on the front panel of the RFSC module should be lit. This sets a positive output voltage for the dynamic disable drive circuits, which simulates the operation of these circuits during body mode.

11. Measure the Direct Drive Output Voltage at TP38. As an upper limit, the voltage should not exceed the voltage measured at TP62. As a lower limit, TP38 voltage should not measure less than TP62 voltage minus 10 volts.

12. Measure the Dynamic Disable Driver output voltages on PIN Switch Driver Board at the following points: Refer to Table 5.

TABLE 5
**DYNAMIC DISABLE DRIVER OUTPUT VOLTAGE CALIBRATION DATA**

| Step | Function | Location (Silk Screen) | Pot. Adj. | Specification |
|---|---|---|---|---|

| | | | | |
|---|---|---|---|---|
| 3-12a | Dyn. Dis. Driver #1 Output Voltage | TP31(W/ TP59) | | Value @ TP62 +0/–10.0 Vdc |
| 3-12b | Dyn. Dis. Driver #2 Output Voltage | TP46 (W/ TP59) | | Value @ TP62 +0/–10.0 Vdc |

**Note**

Voltage Values - Voltage should be no less than the value at TP62 in step 2-8 +0/–10 Vdc.

a. Dynamic Disable Driver # 1 at TP31.

b. Dynamic Disable Driver # 2 at TP46.

c. Move JP5 to Normal Mode (across pins 1 and 2).

## 3- TR DRIVER CIRCUIT ADJUSTMENTS

1. Be sure that T/R-DD Faults Disable switch is off (faults not disabled) on front panel of RFSC module. See Illustration L3167a prior to Section 1.

**CAUTION**

**Possible equipment damage. Do not leave the dynamic disable/TR driver board Jumper JP87 in position C for any extended time. Damage to the phosphorous spectroscopy T/R switch box will occur.**

2. Connect DVM leads to TP16 with respect to TGND (TP59). Move jumper JP87 across pins 1 and 2 (Transmit Simulation, Test Mode "C"). See Illustration L3169a in Section 1. This sets a positive output voltage for the TR driver circuits which simulates the transmit mode.

3. Adjust the loaded TR driver output voltages on PIN Switch Driver Board as shown in Table 6.

TABLE 6
**TR DRIVER CALIBRATION DATA**

| Step | Function | Location (Silk Screen) | Pot. Adj. | Specification |
|---|---|---|---|---|
| 4-3b | TR Driver (Body) (Loaded) | TP16 (W/TP59) | R13 | +4.0 ±0.1 Vdc |
| 4-3d | TR Driver (Head) (Loaded) | TP9 (W/TP59) | R26 | +8.0 ±0.1 Vdc |
| 4-3f | TR Driver (Spectro) (Loaded) | TP21 (W/TP59) | R18 | +4.0 ±0.1 Vdc |

a. Measure the body TR driver output voltage at TP16.

b. Adjust R13 until the voltage at TP16 is +4.0 ±0.1 Vdc. Move jumper JP87 across pins 5 and 6 (software mode).

**NOTE**

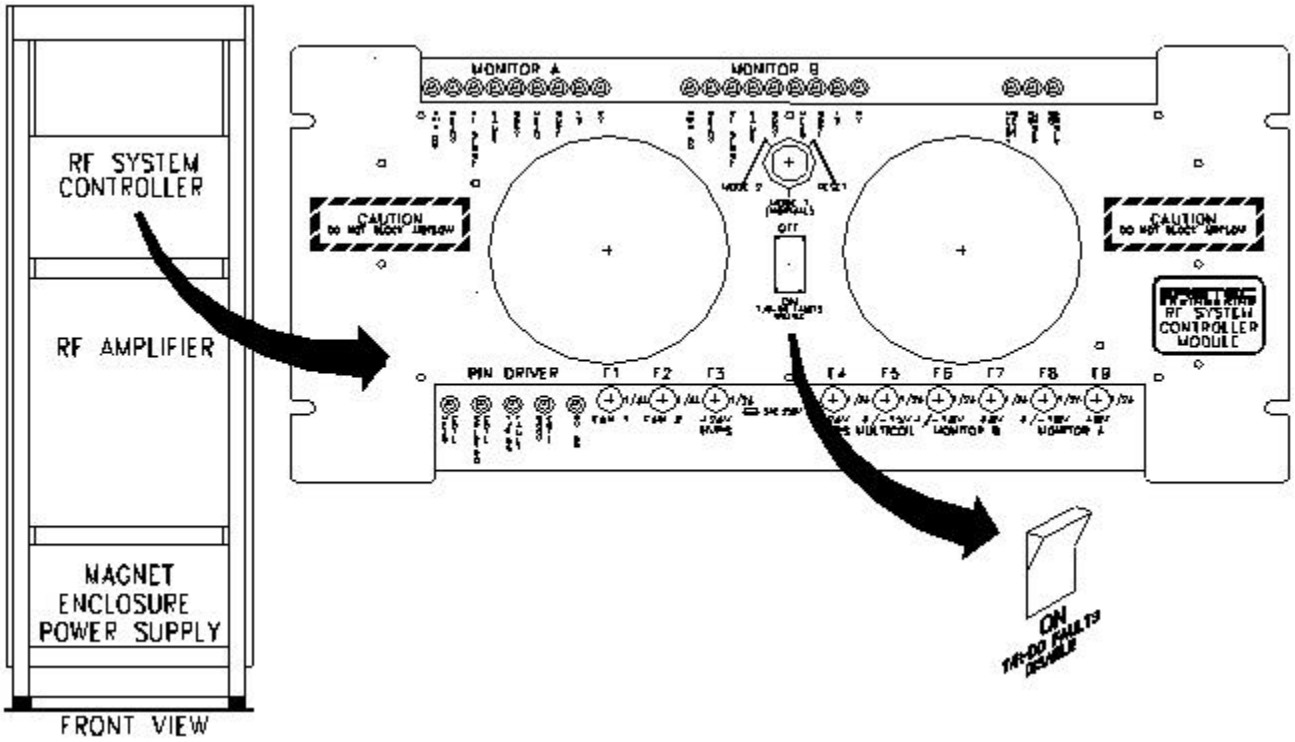
If you are unable to adjust the voltage at TP16 to +4.0 $\pm$ 0.1 Vdc Use the alternate procedure shown on the following two pages as Alternate Procedure 1

ALTERNATE PROCEDURE 1

**ALTERNATE TR DRIVER ADJUSTMENT PROCEDURE**

1. At ISE CERD (MR2A30A13), move switch to "RF Out Disable" to remove excitation from RF amplifier. The switch is located just below jumper J108.

2. Move T/R-DD Faults Disable switch to on position (service mode) on the RFSC module face panel to disable error reporting from the board. See Illustration L3146a.




**DYNAMIC DISABLER / TR DRIVER IN TEST POSITION**
ILLUSTRATION L3146A

3. Set up for a body coil scan, and select the landmark as for a head coil scan.

4. Select [Manual Prescan], then select [Scan TR].

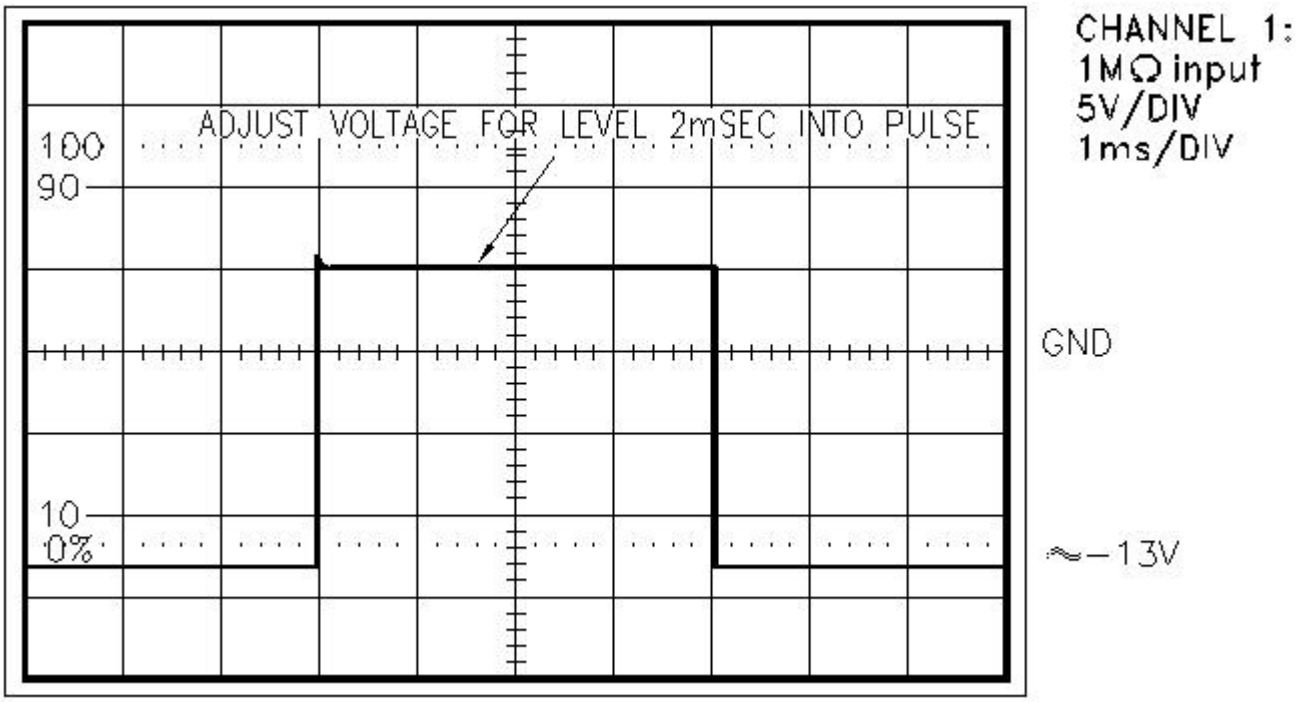
5. Note the ground reference point on the oscilloscope with the scope set to 2V/div.

6. Attach the scope leads to TP16 with respect to TGND (TP59). Trigger the signal that there is one pulse exhibited on the scope.

7. Adjust R13 until the voltage at TP16 is +4.0Vdc $\pm$ 0.5Vdc with respect to the ground reference on the scope. Refer to Table 9 and see Illustration L3170a.

TABLE 9
**TR DRIVER CIRCUIT TEST POINT DYNAMIC MEASUREMENTS**

| Test point | Rating | Tolerance | Function |
|---|---|---|---|
| TP16 | 4.0 Vdc | ± 0.1 Vdc | R13 |
| TP9 | 8.0 Vdc | ± 0.1 Vdc | R26 |
| TP21 | 4.0 Vdc | ± 0.1 Vdc | R18 |




**TR DRIVER CIRCUIT TEST POINT WAVEFORM**
ILLUSTRATION L3170A

8. Next, attach the scope to TP9 with respect to TP59. dust R26 until the voltage at TP9 is +8.0Vdc + 0.5Vdc with respect to the ground reference on the scope, Refer to Table 9.

9. For the Spectro TR adjust, connect the scope leads to TP21 with respect toTP59. Adjust R18 until the voltage reads +4.0Vdc ± 0.5Vdc with respect to the ground reference on the scope, Refer to Table 9.

10. Then continue on with the dynamic operation of the TR Drivers (Step #9).

(End Procedure)

(Section 3 Continued)

c. Connect DVM leads to TP9 with respect to TGND (TP59). Move jumper JP87 across pins 1 and 2 (Transmit Simulation, Test Mode "C"). Measure the Head TR Driver output voltage at TP9.

d. Adjust R26 until the voltage at TP9 is 8.0 ±0.1 Vdc. Move jumper JP87 across pins 5 and 6 (software mode).

**NOTE**

If you are unable to adjust the voltage at TP9 to +8.0 ± 0.1 Vdc Use the alternate procedure shown Alternate Procedure 1 on the previous two pages.

e. Connect DVM leads to TP21 with respect to TGND (TP59). Move jumper JP87 across pins 1 and 2 (Transmit Simulation, Test Mode "C"). Measure the Spectro TR Driver output voltage at TP21.

f. Adjust R18 until the voltage at TP21 is 4.0 ±0.1 Vdc. Move jumper JP87 across pins 5 and 6 (software mode).

**NOTE**

If you are unable to adjust the voltage at TP21 to +4.0 ± 0.1 Vdc Use the alternate procedure shown on the previous two pages.

4. Verify that the loaded TR driver circuit operation on PIN Switch Driver Board as shown in Table 7.

TABLE 7
**TR DRIVER UNLOADED/LOADED CALIBRATION DATA**

| Step | Function | Location (Silk Screen) | Pot. Adj. | Specification |
|---|---|---|---|---|
| 4-4a | TR Driver (Body) (Loaded) | TP13 (W/TP59) | | > Value @ TP12 |
| 4-4b | TR Driver (Head) (Loaded) | TP1 (W/TP59) | | > Value @ TP17 |
| 4-4c | TR Driver (Spectro) (Loaded) | TP18 (W/TP59) | | > Value @ TP19 |

a. Move jumper JP87 across pins 1 and 2 (Transmit Simulation, Test Mode "C"). Verify that the voltage at TP13 is greater than the voltage at TP12, the body TR threshold. Move jumper JP87 across pins 5 and 6 (software mode). The voltage at TP13 is directly proportional to the body TR switch load current: **Current ( I ) of body TR = Voltage of TP13 ÷ 10.** If TP13 is not greater than TP12, recheck measurement at TP12.

b. Move jumper JP87 across pins 1 and 2 (Transmit Simulation, Test Mode "C"). Verify that the voltage at TP1 is greater than the voltage measured at TP17, the head TR threshold. Move jumper JP87 across pins 5 and 6 (software mode). The voltage at TP1 is directly proportional to the head TR switch load current: **Current (I) of head TR = Voltage of TP1 ÷ 10.** If TP1 is not greater than TP17, recheck measurement TP17.

c. Move jumper JP87 across pins 1 and 2 (Transmit Simulation, Test Mode "C"). Verify that the voltage at TP18 is greater than the voltage measured at TP19, the spectroscopy TR threshold. Move jumper JP87 across pins 5 and 6 (software mode). The voltage at TP18 is directly proportional to the Spectro TR switch load current: **Current ( I ) of spectro TR = Voltage of TP18 ÷ 10.** If Spectro TR Switch Box is not installed, then you will read less than 1.0 Vdc due to lack of current draw. If Spectro TR Switch is installed, and TP18 is not greater than TP19, recheck measurement at TP19.

5. Reset any power monitor faults with the key switch.

6. Install JP87 across pins 3 and 4 (Receiver Simulation, Test Mode "B") on the PIN Switch Driver board. See Illustration L3169a in Section 1.

7. Measure and verify test points on the PIN Switch Driver Board. Refer to Table 8.

**Note**

Measurements Should Be Made In Reference To TGND - Although the Dynamic Disable module is grounded to the chassis, all measurements should be made in reference to LGND (TP58, logic ground) on the board, and not to the module chassis, unless otherwise stated. Incorrect measurement readings could occur if chassis is used as the reference.

8. Verify that JP5 is connected across pins 1 and 2 (normal mode), and that JP87 is connected across pins 5 and 6 (software mode), on the PIN Switch Driver board. See Illustration L3168a and Illustration L3169a both in Section 1

9. Verify the dynamic operation of the TR drivers:

a. At ISE CERD (MR2A30A13), move switch to "RF Out Disable" to remove excitation from RF amplifier. The switch is located just below the jumper J108.

b. Move T/R-DD Faults Disable switch to on position (service mode) on the RFSC module face panel to disable error reporting from the board. See Illustration L3146a. in Section 3

c. Set up for a body coil scan, and select the landmark as for a head coil scan.

d. Select **[Manual Prescan]**, then select **[Scan TR]**.

e. Monitor (on an oscilloscope) the TR driver test points corresponding to the output voltages. Refer to Table 9. Verify that voltages are within tolerances at 2 msec after Unblank (see Illustration L3170a in Section 3).

TABLE 9
**TR DRIVER CIRCUIT TEST POINT DYNAMIC MEASUREMENTS**

| Test Point | Rating | Tolerance | Function |
|---|---|---|---|
| TP16 | 4.0 Vdc | ± 0.1 Vdc | R13 |
| TP9 | 8.0 Vdc | ± 0.1 Vdc | R26 |
| TP21 | 4.0 Vdc | ± 0.1 Vdc | R18 |

f. Select **[Pause]**. Move T/R-DD Faults Disable switch to off position. See Illustration L3167a prior to Section 1.

g Select **[Start Scan]**. If TR errors are reported, and TR Switches are verified to be OK, recheck connections to J407, J408, and J409 at the rear of the RFSC module, and verify the sections of the calibration procedure relating to the TR driver circuits.

h. When operation is satisfactory, Select **[Stop Scan]**.

## 4- MULTICOIL DRIVER CIRCUIT ADJUSTMENTS (MULTICOIL SYSTEMS ONLY)

1. Be sure that T/R-DD Faults Disable switch is off (faults not disabled) on PIN Switch Driver board. See Illustration L3167a before Section 1.

2. Position jumpers JP57–60 to pins 1 and 2 (Transmit Simulation, Test Mode "C"). See Illustration L3169b in Section 1. This sets a positive output voltage for the multicoil driver circuits which simulates the transmit mode.

3. Adjust the loaded multicoil driver output voltages on PIN Switch Driver Board as follows: Refer to Table 10.

TABLE 10
**MULTI-COIL DRIVER CALIBRATION DATA**

| Step | Function | Location | Pot. adj. | Specification |
|---|---|---|---|---|
| 5-3b | Multicoil 1 Driver (Loaded) Transmit | TP2 (W/TP59 | R133 | +5.0 ± 0.1Vdc |
| 5-3c | Multicoil 2 Driver (Loaded) Transmit | TP14 (W/TP59) | | +5.0 ± 0.1Vdc |
| 5-3c | Multicoil 3 Driver (Loaded) Transmit | TP20 (W/TP59) | | +5.0 ± 0.1Vdc |
| 5-3c | Multicoil 4 Driver (Loaded) Transmit | TP26 (W/TP59) | | +5.0 ± 0.1Vdc |
| 5-5b | Multicoil 1 Driver (Loaded) Receive | TP2 (W/TP59) | R129 | +5.0 ± 0.1Vdc |
| 5-5c | Multicoil 2 Driver (Loaded) Receive | TP14 (W/TP59) | | +5.0 ± 0.1Vdc |
| 5-5c | Multicoil 3 Driver (Loaded) Receive | TP20 (W/TP59) | | +5.0 ± 0.1Vdc |
| 5-5c | Multicoil 4 Driver (Loaded) Receive | TP26 (W/TP59) | | +5.0 ± 0.1Vdc |

a. Measure the multicoil 1 driver output voltage at TP2 with respect to TGND (TP59).

b. Adjust R133 until the voltage at TP2 is +5.0 ± 0.1 Vdc.

c. Check multicoil 2, 3, 4 driver outputs at TP14, 20, 26, respectively, to ensure that they are at +5.0 ±0.1 Vdc.

4. Move jumpers JP57–60 to pins 3 and 4 (Receive Simulation Mode "B"). See Illustration L3169b in Section 1.

5. Adjust the multicoil driver output voltage on PIN Switch Driver Board as shown in Table 10 above.

   a. Measure the multicoil 1 driver output at TP2 with respect to TGND (TP59).

   b. Adjust R129 until voltage at TP2 is –5.0 ±0.1 Vdc.

   c. Check multicoil 2, 3, 4 driver outputs at TP14, 20, 26 respectively to ensure that they are at –5.0 ± 0.1 Vdc.

6. Verify that the loaded Multicoil Driver Error Detection circuit operation on PIN Switch Driver Board as shown in Table 11.

TABLE 11
**MULTICOIL DRIVER/LOADED ERROR DETECTION DATA (TRANSMIT MODE)**

| Step | Function | Location | Pot. adj. | Specification |
|---|---|---|---|---|
| 5-6a | Multicoil 1 Driver (Loaded) | TP7 (W/TP59) | | <TP8 |
| 5-6b | Multicoil 2 Driver (Loaded) | TP11 (W/TP59) | | <TP3 |
| 5-6c | Multicoil 3 Driver (Loaded) | TP22 (W/TP59) | | <TP25 |
| 5-6d | Multicoil 4 Driver (Loaded) | TP28 (W/TP59) | | <TP24 |

   a. Install a four-coil array (CTL coil recommended, Pelvic Array not acceptable). If a four-coil array is not available, verify that voltages at TP7, TP11, TP22, and TP28 are between –1.4 Vdc and –2.0 Vdc (unloaded value).

**Note**

Two-channel Multicoil Setup - For a two-channel multicoil option, if a CTL coil is not available, use the Body Flex coil with the Dual Phased Array Adapter instead of the CTL coil. Then adjust only multicoil channel 1 and 3 under the load condition. Do not attempt to adjust multicoil channels 2 and 4 under load conditions.

   b. When jumpers JP57–60 are configured for transmit mode (across pins 1 and 2), verify that the voltage at TP7 is less than the voltage at TP8. The voltage at TP7 is directly proportional to the multicoil 1 load current: **Current (I) of Multicoil 1 = Voltage of TP7 ÷ 5**. If TP7 is not less than the voltage at TP8, recheck measurements at TP8.

   c. When jumpers JP57–60 are configured for transmit mode (across pins 1 and 2), verify that the voltage at TP11 is less than the voltage at TP3. The voltage at TP11 is directly proportional to the multicoil 2 load current: **Current (I) of Multicoil 2 = Voltage of TP11 ÷ 5**. If TP11 is not less than the voltage at TP3, recheck measurements at TP3.

d. When jumpers JP57–60 are configured for transmit mode (across pins 1 and 2), verify that the voltage at TP22 is less than the voltage at TP25. The voltage at TP22 is directly proportional to the multicoil 3 load current: **Current (I) of Multicoil 3 = Voltage of TP22 ÷ 5**. If TP22 is not less than the voltage at TP25, recheck measurements at TP25.

e. When jumpers JP57–60 are configured for transmit mode (across pins 1 and 2), verify the voltage at TP28 is less than the voltage at TP24. The voltage at TP28 is directly proportional to the multicoil 4 load current: **Current (I) of Multicoil 4 = Voltage of TP28 ÷ 5**. If TP28 is not less than the voltage at TP24, recheck measurements at TP24.

7. Verify that the loaded multicoil driver error detection circuit operation on PIN Switch Driver Board as shown in Table 12. (Keep the same coil connected as in the previous step.)

TABLE 12
**MULTI-COIL DRIVER/LOADED ERROR DETECTION DATA (RECEIVE MODE)**

| Step | Function | Location | Pot. adj. | Specification |
|---|---|---|---|---|
| 5-7a | Multicoil 1 Driver (Loaded) | TP7 (W/TP59) | | <TP10 and >TP8 |
| 5-7b | Multicoil 2 Driver (Loaded) | TP11 (W/TP59) | | <TP4 and >TP3 |
| 5-7c | Multicoil 3 Driver (Loaded) | TP22 (W/TP59) | | <TP23 and >TP25 |
| 5-7d | Multicoil 4 Driver (Loaded) | TP28 (W/TP59) | | <TP27 and >TP24 |

a. When jumpers JP57–60 are configured for receive mode (across pins 3 and 4), verify that the voltage at TP7 is less than the voltage at TP10, but greater than the voltage at TP8. The voltage at TP7 is directly proportional to the multicoil 1 load current: **Current (I) of Multicoil 1 = Voltage of TP7 ÷ 5**. If TP7 is not between these voltages, recheck measurements at TP10 and TP8.

b. When jumpers JP57–60 are configured for receive mode (across pins 3 and 4), verify the voltage at TP11 is less than the voltage at TP4, but greater than the voltage at TP3. The voltage at TP11 is directly proportional to the multicoil 2 load current: **Current (I) of Multicoil 2 = Voltage of TP11 ÷ 5**. If TP11 is not between these voltages, recheck measurements at TP3 and TP4.

c. When jumpers JP57–60 are configured for receive mode (across pins 3 and 4), verify that the voltage at TP22 is less than the voltage at TP23, but greater than the voltage at TP25. The voltage at TP22 is directly proportional to the multicoil 3 load current: **Current (I) of Multicoil 3 = Voltage of TP22 ÷ 5**. If TP22 is not between these voltages, recheck measurements at TP25 and TP23.

d. When jumpers JP57–60 are configured for receive mode (across pins 3 and 4), verify the voltage at TP28 is less than the voltage at TP27, but greater than the voltage at TP24. The voltage at TP28 is directly proportional to the multicoil 4 load current: **Current (I) of Multicoil 4 = Voltage of TP28 ÷ 5**. If TP28 is not between these voltages, recheck measurements at TP24 and TP27.

8. Reset any power monitor faults with the key switch.

9. Verify that jumpers JP–60 on the PIN Switch Driver Board are across pins 5 and 6 (software control mode normal) for four-channel multicoil systems, or **across pins 3 and 4 Receive mode B for nonmulticoil systems.** For two-channel multicoil systems, verify that JP57 and JP59 are in software control mode (normal mode, pins 5 and 6 connected), and that JP58 and JP60 are in B mode (receive mode, pins 3 and 4 connected). See Illustration L3169b in Section 1.

## 5- RESTORATION CHECK LIST

1. Replace the rear shield on the top of the RFSC module.

2. At ISE CERD (MR2A30A13), move toggle switch to RF Out Normal for excitation to RF amplifier.

3. Verify that jumper JP87 is across pins 5 and 6 (software mode), and that JP5 is across pins 1 and 2 (normal mode).

4. Verify that jumpers JP57–60 on the PIN Switch Driver Board are across pins 5 and 6 (software control mode normal) for four-channel multicoil systems, or across pins 3 and 4 Receive Mode B for nonmulticoil systems. For two-channel multicoil systems, verify that JP57 and JP59 are in software control mode (normal mode, pins 5 and 6 connected), and that JP58 and JP60 are in B mode (receive mode, pins 3 and 4 connected). See Illustration L3169b in Section 1.

## 6- QUICK REFERENCE TABLE

**CAUTION**

**Possible equipment damage. Do not use the quick reference table (14) unless you have used the full pin switch driver board adjustment procedure successfully at least twice. This reference table does not provide all information needed. It is a quick reference for field engineers who are familiar with the pin switch driver board adjustment procedure.**

TABLE 14
**PIN SWITCH DRIVER BOARD QUICK REFERENCE TABLE**

1. Verify: T/R-DD Faults Disable switch is off.
   JP57–60 are in Normal Mode (pins 5 & 6) for 4-channel multicoil or
   JP57–60 are in Receive Mode (pins 3 & 4) for nonmulticoil or
   JP57 & JP59 are in Normal Mode (pins 5 & 6) and JP58 & JP60 are in Receive Mode (pins 3 & 4) for 2-channel multicoil.
   JP87 is in Normal Mode (pins 5 & 6).
   JP5 is in Test Mode (pins 2 & 3) & JP6 is in Dynamic & Direct Drive Enable, Test Mode B (pins 1 & 2).
   JP3 is in High Pass Mode (pins 2 & 3).

JP1 is in 1000V Mode for 1.5T system or 500V Mode for 1.0T system.

2 Measure and verify the following outputs of test points: (LGND, TP58) (Verify that the High Voltage Interlock Switch is pulled up to enable the high voltage.)

| Step | Function | Location | Pot. Adj. | Meas. Value | Specification |
|---|---|---|---|---|---|
| 2-8 | –15 V_A Power Supply | TP56 | | | |
| 2-8 | +15 V_A Power Supply | TP51 | | | |
| 2-8 | +5 Vdc Power Supply | TP54 | | | +5.0 ± 0.25 Vdc |
| 2-8 | –15 Vdc Power Supply | TP57 | | | -15.0 ± 0.2 Vdc |
| 2-8 | +15 Vdc Power Supply | TP55 | | | +15.0 ± 0.2 Vdc |
| 2-8 | +500/1000 Vdc Power Supply | TP62 | | | +500 ± 25 Vdc<br>+1000 ± 50 Vdc |

3. Verify:
JP6 is in Dynamic & Direct Drive Disable, Test Mode C (pins 2 & 3).

4. Measure, adjust (where noted), and verify the following outputs of test points:

| Step | Function | Location | Pot. Adj. | Meas. Value | Specification |
|---|---|---|---|---|---|
| 3-3a | Direct Drive Output (J402 Connected) | TP40 (W/TP56) | | | 1.1 ± 0.2 Vdc |
| 3-4a | Dyn. Dis. Driver #1 (J403 Connected) | TP32 (W/TP56) | | | +1.0 ± 0.2 Vdc |
| 3-5a | Dyn. Dis. Driver #2 (J401 Connected) | TP49 (W/TP56) | | | +1.0 ± 0.2 Vdc |
| 3-6 | Direct Drive Output Voltage | TP38 (W/TP59) | | | –2.5 ± 1.0 Vdc (FIXED) |
| 3-7a | Dyn. Dis. Driver #1 (Loaded) | (W/TP59) | | | –5.0 ± 1.5 Vdc (FIXED) |
| 3-7b | Dyn. Dis. Driver #2 (Loaded) | TP46( W/TP59) | | | –5.0 ± 1.5 Vdc (FIXED) |
| 3-8 | Direct Drive Open Circuit Detect | TP44 (W/TP59) | R207 | | Value @ TP45 3.0 ± 0.1 Vdc (Rev. B Body Hybrid) |
| | | | | | Value @ TP45 –2.0 ± 0.1 Vdc (Normal) |
| 3-8 | Dyn. Dis. Driver #1 Open Cir. Detect. | TP34 (W/ TP59) | R147 | | Value @ TP33 -3.0 ± 0.1 Vdc (Rev. B Body Hybrid) |
| | | | | | Value @ TP33 –2.0 ± 0.1 Vdc (Normal) |
| 3-8 | Dyn. Dis. Driver #2 Open Cir. Detect | TP48 (W/ TP59) | R228 | | Value @ TP47–3.0 ± 0.1 Vdc (Rev. B Body Hybrid) |
| | | | | | Value @ TP47 –2.0 ± 0.1 Vdc (Normal) |

5. Verify:JP6 is in Dynamic & Direct Drive Enable, Test Mode B (pins 1 & 2).

6. Measure and verify the following outputs of test points:

| Step | Function | Location | Pot. Adj. | Meas. Value | Specification |
|---|---|---|---|---|---|
| 3-11 | Direct Drive Output Voltage | TP38 | | | Value @ TP62+ 0/–10.0 Vdc |
| 3-12a | Dyn. Dis. Driver #1 Output Voltage | TP31 | | | Value @ TP62+0/–10.0 Vdc |
| 3-12b | Dyn. Dis. Driver #2 Output Voltage | TP46 | | | Value @ TP62 +0/–10.0 Vdc |

7. Verify: JP5 is in Normal Mode (pins 1 & 2).

8. Connect DVM leads to each of the following test points, move JP 87 to Transmit, Test Mode "C" (pins 1 & 2), adjust the potentiometer, if necessary, then move JP 87 to Normal Mode (pins 5 & 6) for each step:

| Step | Function | Location | Pot. adj. | Meas. Value | Specification |
|---|---|---|---|---|---|
| 4-3b | TR Driver (Body) (Loaded) | TP16 (W/TP59) | R13 | | +4.0 ± 0.1 Vdc |
| 4-3d | TR Driver (Head) (Loaded) | TP9 (W/TP59) | R26 | | +8.0 ± 0.1 Vdc |
| 4-3f | TR Driver (Spectro) (Loaded) | TP21 (W/TP59) | R18 | | +4.0 ± 0.1 Vdc |
| 4-4a | TR Driver (Body) (Loaded) | TP13 (W/TP59) | | | > Value @ TP12 |
| 4-4b | TR Driver (Head) (Loaded) | TP1 (W/TP59) | | | > Value @ TP17 |
| 4-4c | TR Driver (Spectro) (Loaded) | | | | > Value @ TP19 |

9. Reset any Power Monitor faults, verify that JP87 is in Receive, Test Mode B (pins 3 & 4).

10. Measure and verify the following test points: (W/TP59)

| Step | Function | Location | Pot. Adj. | Meas. Value | Specification |
|---|---|---|---|---|---|
| 4-7 | Head TR Current Output | TP1 | | | 0.0 ± 0.1 Vdc |
| 4-7 | Head TR Voltage Output | TP9 | | | –13.75 ± 1.5 Vdc |
| 4-7 | Body TR Current Output | TP13 | | | 0.0 ± 0.25 Vdc |
| 4-7 | Body TR Voltage Output | TP16 | | | –13.75 ± 1.5 Vdc |
| 4-7 | Spectro TR Current Output | TP18 | | | 0.0 ± 0.25 Vdc |
| 4-7 | Spectro TR Voltage Output | TP21 | | | –13.75 ± 1.5 Vdc |

11. Verify that JP5 is in Normal Mode A (pins 1 & 2), and that JP87 is in Normal Mode (pins 5 & 6).

12. Verify the dynamic operation of the TR Drivers:
    a. At ISE CERD (MR2A30A13), move switch to RF Out Disable to remove excitation from RF amplifier.

    b. Move T/R-DD Faults Disable switch to On position (service mode) on the PIN Switch Driver Board to disable error reporting from the board (Illustration 2-1).

    c. Set up for a body coil scan and select the landmark as for a head coil scan.

    d. Select **[Manual Prescan]**, then press **[Scan TR]**.

e. Monitor (on an oscilloscope) the TR Driver test points corresponding to the following output voltages: (Verify voltages are within tolerances at 2 msec after Unblank (Illustration L3170a in Section 3).

| Step | Function | Location | Pot. Adj. | Meas. Value | Specification |
|---|---|---|---|---|---|
| 4-9e | TR Driver Circuit | TP16 | R13 | | +4.0 ±0.5 Vdc |
| 4-9e | TR Driver Circuit | TP9 | R26 | | +8.0 ±0.5 Vdc |
| 4-9e | TR Driver Circuit | TP21 | R18 | | +4.0 ±0.5 Vdc |

f. Select **[Pause]**. Return T/R-DD Faults Disable switch to the off position on the PIN Switch Driver Board (Illustration L3167a before Section 1).

g. Select **[Start Scan]**. If TR errors are reported, and TR switches are verified to be OK, recheck connections to J407, J408 and J409 at the rear of the RFSC Module, and verify the sections of the calibration procedure relating to the TR Driver circuits.

h. When operation is satisfactory, select **[Stop Scan]**.

13. Verify:
    T/R-DD Faults Disable switch to the off position.
    JP57–60 are in Transmit, Test Mode C (pins 1 & 2).

14. Adjust the Multicoil Driver output voltage as follows:

| Step | Function | Location | Pot. Adj. | Meas. Value | Specification |
|---|---|---|---|---|---|
| 5-3b | Multicoil 1 (Loaded) Transmit) | TP2 (W/TP59) | R133 | | +5.0 ±0.1 Vdc |
| 5-3c | Multicoil 2 (Loaded) Transmit) | TP14 (W/TP59) | | | +5.0 ±0.1 Vdc |
| 5-3c | Multicoil 3 (Loaded) Transmit) | TP20 (W/TP59) | | | +5.0 ±0.1 Vdc |
| 5-3c | Multicoil 4 (Loaded) Transmit) | TP26 (W/TP59) | | | +5.0 ±0.1 Vdc |

15. Verify: JP57 - JP60 are in Receive, Test Mode B (pins 3 & 4).

16. Adjust the Multicoil Driver output voltage as follows:

| Step | Function | Location | Pot. Adj. | Meas. Value | Specification |
|---|---|---|---|---|---|
| 5-5b | Multicoil 1 (Loaded) (Receive) | TP2 (W/TP59) | R129 | | -5.0 ±0.1 Vdc |
| 5-5c | Multicoil 2 (Loaded) (Receive) | TP14 (W/TP59) | | | –5.0 ±0.1 Vdc |
| 5-5c | Multicoil 3 (Loaded) (Receive) | TP20 (W/TP59) | | | –5.0 ±0.1 Vdc |
| 5-5c | Multicoil 4 (Loaded) (Receive) | TP26 (W/TP59) | | | –5.0 ±0.1 Vdc |

17. Install a 4-channel Phased Array coil (or 2-channel Phased Array coil, if 2-channel multicoil system).

18. Verify:JP57 - JP60 are in Transmit, Test Mode C (pins 1 & 2).

19. Verify that the voltages are as specified in the following:

| Step | Function | Location | Pot. Adj. | Meas. Value | Specification |
|---|---|---|---|---|---|
| 5-6b | Multicoil 1 Error Detect (Loaded) (Transmit) | TP7 (W/TP59) | | | <TP8 |
| 5-6c | Multicoil 2 Error Detect (Loaded) (Transmit) | TP11 (W/TP59) | | | <TP3 |
| 5-6d | Multicoil 3 Error Detect (Loaded) (Transmit) | TP22 (W/TP59) | | | <TP25 |
| 5-6e | Multicoil 4 Error Detect (Loaded) (Transmit) | TP28 (W/TP59) | | | <TP24 |

20. Verify:JP57 - JP60 are in Receive, Test Mode B (pins 3 & 4).

21. Verify that the voltages are as specified in the following:

| Step | Function | Location | Pot. Adj. | Meas. Value | Specification |
|---|---|---|---|---|---|
| 5-7a | Multicoil 1 Error Detect (Loaded) (Receive) | TP7 (W/TP59) | | | <TP10 and >TP8 |
| 5-7b | Multicoil 2 Error Detect (Loaded) (Receive) | TP11 W/TP59) | | | <TP4 and >TP3 |
| 5-7c | Multicoil 3 Error Detect (Loaded) (Receive) | TP22 W/TP59) | | | <TP23 and >TP25 |
| 5-7d | Multicoil 4 Error Detect (Loaded) (Receive) | TP28 W/TP59) | | | <TP27 and >TP24 |

22. Reset any power monitor faults.

23. Verify:
    a. Replace the rear shield on the top of the RF System Controller Module.

    b. At ISE CERD (MR2A30A13), move switch to RF Out Normal for excitation to RF amplifier.

    c. Verify jumpers JP87 is across pins 5 & 6 (Software Control, Normal Mode A and JP5 is across pins 1 & 2 (Software Control, Normal Mode A).

    d. Verify that jumpers JP57–60 on the PIN Switch Driver Board are across pins 5 & 6 (Software, Normal Mode A) for 4-channel multicoil systems or across pins 3 & 4 Receive, Test Mode B for nonmulticoil systems. For two-channel multicoil systems, verify thatJP57 & JP59 are in (Software, Normal Mode A, pins 5 & 6 connected) and JP58 & JP60 are in Test Mode B (Receive Mode, pins 3 & 4 connected). See Illustration L3169a in Section 1.

# REVISION HISTORY

| REV | DATE | AUTHOR | PRIMARY REASONS FOR CHANGE |
|---|---|---|---|
| 0 | July 24, 1998 | J. Saperstein | Initial conversion from Toolbook to Word. |
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