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GRADIENT DRIVER THEORY - SGD HI SLEW CABINET

1- GRADIENT INTERFACE PROCESSOR (GIP)

The Gradient Interface Processor (GIP) circuit board shall provide an intelligent interface between the Signa or Lightning Systems Cabinets, and the Scaleable Gradient Driver (SGD).

All SGD hardware shall be controlled from the GIP. The Systems Cabinet (or suitable test equipment) is required to command the system to ready and report errors. Handshaking between power electronics modules will be done in hardware on the GIP to ensure that all power hardware is disabled if a fault occurs. The GIP will provide an analog drive signal for the Gradient Power Modules (GPMs) and mini-GRAMS (mGRAMs), as well as a power supply level input to the GRAM Power Supply (mGRAM-PS). The GIP shall also perform the functions of the Analog Service Module (ASM) by sampling various analog signals on the power electronics modules, and presenting them to the system for fault detection and analysis.

Gradient amplifier data is transmitted from the TYME (or TYME II) to the GIP over 4 high speed fiber optic cables. Three of these cables carry 21 bit serial data (X, Y, and Z), the fourth carries a gated 10 MHz clock (CLK). New gradient data is shifted out once every 4 μsec. For each data burst, the GIP shall capture the serial data stream and check for framing errors. That data will then be shifted out to the GIP DACs on the next 21 bit data burst. In parallel with the gradient data updates, the GIP processor shall monitor the status of the gradient amplifiers and respond appropriately. Fault conditions shall be handled locally or communicated to IPG via the MDS link.

DSP PROCESSOR

The TMS320C31-40 Digital Signal Processor shall be the main processor on the GIP. It shall run at 40 MHz out of zero wait state external RAM. Upon power-up, the TMS320C31 shall boot-load out of Flash EPROM.

1- GRADIENT INTERFACE PROCESSOR (GIP) (continued)

HSSD FIBER OPTIC INPUTS (GRADIENT DATA)

Four 820 nm optical inputs shall be provided to the GIP. One of these signals (CLK) is a 10Mhz clock burst that will not occur more frequently than once every 4 μsec. The remaining three signals (X, Y, and Z) are 21 bit serial data streams, one for each axis of the Gradient Amplifier subsystem. The GIP shall convert these optical inputs to TTL level defined signals.

The optical receiver input power shall be :

Receiver	ON	OFF
Gradient Data Receivers	≥-24dBm	≤-40dBm

HSSD INTERFACE TIMING REQUIREMENTS
ILLUSTRATION 1-1

ERROR DETECTION (GRADIENT DATA FROM SYSTEMS CABINET)

Gradient data is shifted into the GIP via CLK. Hardware shall detect two types of errors on the incoming CLK signal:

A Framing Error shall be reported if exactly 21 clock pulses are not received in a clock burst. A framing error condition is defined when both T_{clk} > 200nsec AND N ≠ 21. See Figure 4.2.4.

A Clock Stop error shall be reported if a clock signal is not detected for a time interval exceeding 32μS. A clock stop error condition is defined when T_{frame} > 32 μsec. See Figure 4.2.4.

Error detection by hardware shall not be provided for the X, Y, and Z data streams.

If an error is NOT detected, the received data shall be shifted out to the Gradient Amplifiers on the next clock burst. If a framing error IS detected, the GIP hardware shall suspend gradient updates until a valid frame is received. If a clock-stop error is detected, both the current and derivative DACs shall be loaded with zeros. Upon either error condition, the error detection circuit shall also notify the DSP through Framing Error or Clock Stop Registers. Upon power-up or reset, the GIP hardware shall suspend gradient updates until a valid clock frame is received.

GRADIENT COMMAND DATA SAMPLING (SYSTEMS MODE)

Every 4 μsec, the GIP shall latch X, Y, and Z gradient data coming from IPG into hardware registers. This data shall be latched synchronous to INT0*. When the DSP services INT0*, it shall transfer the X, Y, and Z gradient data values into RAM. INT0* is only active in Systems Mode.

1- GRADIENT INTERFACE PROCESSOR (GIP) (continued)

Every 4 μsec, the GIP hardware shall sample and interpret the 21st bit of the X, Y, and Z gradient data streams. This bit shall represent the PSD-PWM-ON command from the PSD. Refer to section 4.2.9 for the interpretation of this bit.

The GIP shall power up in the Systems Mode.

GRADIENT DATA UPDATE REGISTER (LOCAL MODE)

A diagnostic mode (Local Mode) shall be provided to allow the GIP to exercise the amplifiers independent of a complete system. In this mode, the normal gradient data flow through the board is suppressed and the data driven to the amplifiers shall originate from a register updated by the GIP's DSP. Gradient updates shall occur every 32 μsec synchronous to INT2*. When the DSP services INT2*, it shall update the gradient update register with the next data value to be written to the selected amplifier axis. To operate in this mode, the DSP shall configure the SELECT bits for Local Mode. The DSP shall also configure the mGRAMs in Freewheel mode for local updates (due to the 32 μsec timing). If the SELECT bits are configured for System Mode, gradient data updates are executed as described in 4.2.5.

CURRENT DAC (*I*) OUTPUT

Delay from the start of the HSSD packet to the start of the Icoil stimulus shall be TBD. SNR shall be 110dB minimum. Resolution shall be 20-bits. The gain of this circuit shall be 1V=50A. The offset of this circuit shall be adjustable to less than ±10mV.

1- GRADIENT INTERFACE PROCESSOR (GIP) (continued)

DERIVATIVE DAC (*dI/dt*) OUTPUT

Hardware on the GIP shall calculate the derivative of the incoming waveforms (based on a fixed 4μs *dt*), and shall drive the mGRAM with this signal. If the difference between two consecutive data values is beyond the mathematical capabilities of the GIP, an over-range warning bit shall be set in a register. Under these conditions, the GIP shall suspend the update to the mGRAM, and the mGRAM will hold its output at the "last good" value, until a valid derivative is calculated.

Monotonicity shall be guaranteed to 12-bits. Resolution shall be 12-bits. The gain of this circuit shall be 1V=200V. The offset of this circuit shall be adjustable to less than ±10mV.

FREEWHEEL COMMAND

The freewheel command is based upon four inputs: the 21st bit, (which is sent independently for each axis), the mask (which controls whether the 21st bit is interpreted or ignored), the PWM-On-Calc signal (a calculation which determines if a ramp is in process), and the Force FW register, (which disables mGRAM PWM operation). The mask may be set by the GIP according to an opcode from the SPI.

DIGITAL TUNING

The Digital Tuning section of the GIP board will allow the system to control eddy current compensation and LCOIL signals on each axis. (Loop Gain will be a fixed resistor and will not be adjustable). Seven passive first-order high-pass filters make up the eddy-current compensation on the GIP.

The digital tuning circuit is not required to retain any settings when power is removed. All adjustments shall be re-established upon power-up or reset of the GIP. The GIP processor shall have access to 6 registers for digital tuning.

LCOIL ADJUSTMENT

The LCOIL circuit shall control the gain and DC offset from the derivative DAC output. The offset shall be a manual (factory) setting. The gain shall be controlled using a 12-bit multiplying DAC, or by a manual pot adjustment.

LOOP GAIN ADJUSTMENT2

The gain of the GRAM current loop regulator shall be set with a fixed resistor and is not adjustable.

CURRENT MONITOR OUTPUT

The GIP shall provide a buffered version of each amplifier current at a BNC connector on the front panel. The scale shall be 1V/50A, (+/-5V full scale) and shall be accurate to $\pm$ 3%.

1- GRADIENT INTERFACE PROCESSOR (GIP) (continued)

DUART

A DUART shall be provided to interface the DSP processor to an RS-232 debug port and a duplex fiber optic serial port (MDS link). The DUART shall interrupt the processor when activity occurs on either channel.

Additionally, the DUART's output pins shall be used to control a variety of functions. These functions include gradient update mode selection (local vs. system), control of the processor status LED, MDS loopback control, and debug test nodes. The DUART's input pins shall be used by software to read the board revision and to determine if a debug terminal is connected.

MDS (MULTI-DROP SERIAL) INTERFACE

Fiber Optic devices shall be provided to interface the DUART to the MDS Link. A break character detect circuit shall be provided to reset the processor if the data line is held active for 15 characters (at 9600 Baud). The DUART shall interrupt the DSP if any relevant data comes into the GIP and the DSP shall control all data traffic leaving the GIP. Loopback control shall also be provided to loopback MDS data onto the MDS link.

The optical output power shall be:

Transmitter	ON	OFF
MDS	≥-17dBm	≤-40dBm

The optical receiver input power shall be :

Receiver	ON	OFF
MDS	≥-24dBm	≤-40dBm

DEBUG TERMINAL PORT

An RS-232 interface shall be provided to connect to a debug terminal. RXD, TXD, and DTR signals shall be used.

STATIC RAM

128k x 32 zero wait state static RAM shall be provided for program space and waveform storage.

FLASH EPROM

256k x 8 Flash EPROM shall be provided to boot load the processor. A 16k boot block shall be provided that will provide the GIP with basic functionality. A jumper shall be provided to prevent accidental erasure of this block. The EPROM shall be pre-programmed before board assembly to provide initial functionality.

1- GRADIENT INTERFACE PROCESSOR (GIP) (continued)

SGD MODULE INTERFACE (STATUS AND CONTROL)

The GIP shall be the master of eight separate Real-Time Interfaces, one interface for each GPM axis, one for each mGRAM axis, one for the GPM-PS, and one for the mGRAM-PS. This interface allows the GIP to configure and monitor the power electronics hardware. All enable and fault handshaking shall be provided on the GIP. Thus, in the event of an error, the GIP hardware will disable all power electronics in addition to notifying the DSP of the event. The DSP shall have individual enable control over each module.

Digital status and control signals shall have ≥ 300V common mode isolation and use ≅ 100Ω termination. Digital status signals shall be capable of driving into 100Ω line impedance. Analog signals shall be driven and received in a balanced differential manner. Common-mode chokes are to be part of the analog receiver circuit for Icoil. Signals shall be appropriately filtered to minimize susceptibility to high-frequency noise and glitches.

ASM INTERFACE (ADC DATA)

This interface will sample GPM, Power Supply, and mGRAM temperature, current, and voltage data, and return these values to the DSP for processing. Signal selection shall be accomplished in hardware according to a hardware selection register. When ASM data is valid on the GIP, an external interrupt (INT2*) will be generated so that the DSP can transfer this data into RAM.

The ASM data shall be buffered such that the DSP can access the data registers up to 31μs after INT2. ASM data shall be valid within one INT2 cycle (32μs) after changing the MUX select bits.

A maximum of four signals shall be acquired simultaneously from the ASMs. The combinations of the ASM signals have been correlated to Gradient Subsystem Diagnostics.

2- GRADIENT POWER MODULE (GPM, 8651)

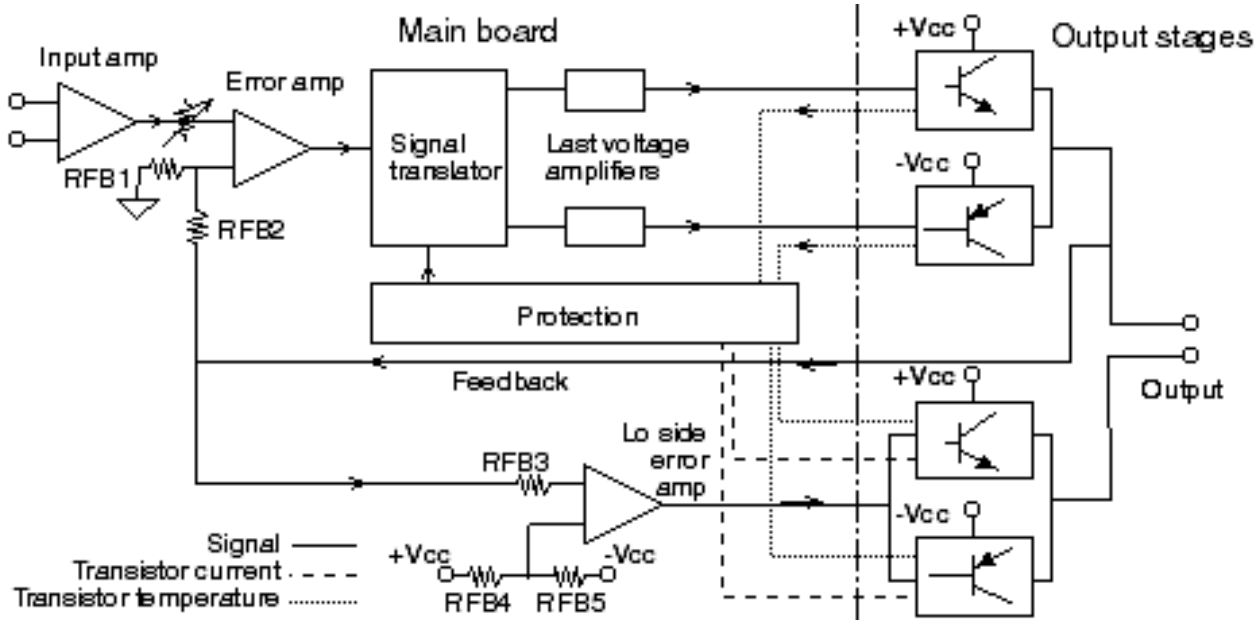
The 8651 Gradient Power Module is a three channel, voltage mode power amplifier. All channels are identical to each other in design and capabilities. The purpose of the 8651 is to amplify a low voltage, analog signal from the GIP and drive the gradient field coils.

Each amplifier is composed of three major components, the main board, the output shelf and a poly phase buck module. In addition to these components, an external dc supply and forced air cooling system is required to operate the 8651.

All sections of the 8651 operate inside of a closed loop system consisting of the GIP, the 8651 and GRAM. The GIP develops the analog waveform, and sends it to the 8651 which amplifies the voltage.

CIRCUIT PRINCIPLES

Illustration 2-1 below is the block diagram of the 8651. Power supplies are not included in this block diagram.



CLOSED LOOP FEEDBACK
ILLUSTRATION 2-1

Each amplifier is a bridge of four power amplifier elements powered by a floating supply. The 8561 is built around a voltage amplifier which first drives the high side of the bridge. The low side of the bridge is in turn driven from the high side such that one half of the voltage of the output signal is imposed on the Vcc supply rails. Feedback, although not shown in all locations, is used liberally to acquire the control of the bridge balance and insure the required overall linearity.

2- GRADIENT POWER MODULE (GPM, 8651) (continued)

INPUT AMPLIFIER

The first stage in the 8651 is the input amplifier. This stage receives the differential analog signal via J100 (located on the main board) or J200 (located on the back panel). The input amplifier converts the balanced signal generated by the GIP and converts it to an unbalanced signal to drive the error amplifier. Jumpers on the main board disconnect J200 from the input amplifier. This stage is outside of the amplifier's main feedback loop.

ERROR AMPLIFIER

The unbalanced signal from the input amplifier is adjusted by R158 and then drives the error amplifier. This stage is a high performance op-amp that forms the feedback loop around the power amplifier. Two precision resistors set the gain to 20.

SIGNAL TRANSLATOR

The output of the error amplifier drives the signal translator stage. This stage is composed of several transistors that provide a balanced signal to the last voltage amplifiers. Supply current for the signal translator is controlled by the protection circuitry.

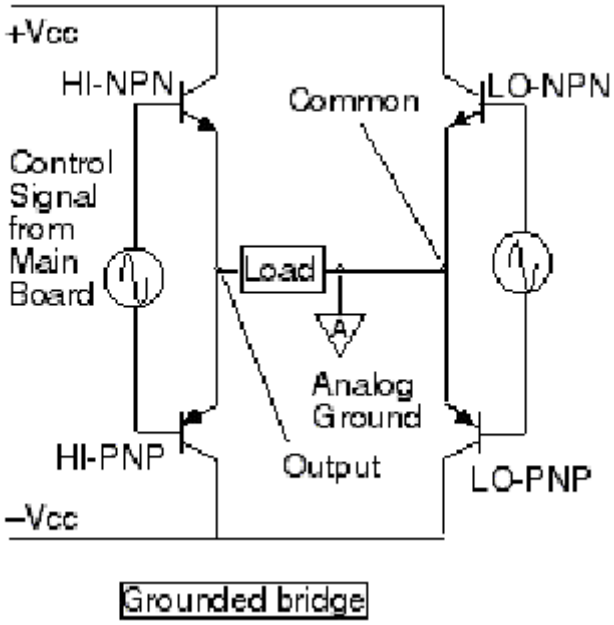
LAST VOLTAGE AMPLIFIER

Drive to the high side of the output stages of the 8651 comes from the last voltage amplifier. This stage provides voltage amplification to the output of the signal translator. The last voltage amplifier transistors are current limited which controls the slew limit of the amplifier in that the load to the stage is dominated by capacitance in the output stage.

2- GRADIENT POWER MODULE (GPM, 8651) (continued)

OUTPUT STAGES

The 8651 uses a full bridge output stage to direct-couple the amplifier to make full use of the available supply voltage as the peak output to the load is 2 Vcc. See Illustration 2-2.



OUTPUT STAGES
ILLUSTRATION 2-2

The peak-to-peak output voltage of the full bridge is actually twice the available supply voltage (4 Vcc). The maximum voltage stress to the output stage devices is the same as in the totem-pole topology (2 Vcc). The supply use is now total.

The low sides are connected to the circuit ground, and the HI sides are connected to the output. Even though each final stage consists of 20 NPN power transistors wired in parallel, the quadrants are named PNP (or NPN) because they act as if they were a single giant PNP (or NPN) transistor. For positive current to flow through the load, the HI-NPN and the LO-PNP quadrants conduct current. For negative current to flow through the load, the HI-PNP and LO-NPN quadrants conduct current.

2- GRADIENT POWER MODULE (GPM, 8651) (continued)

OUTPUT STAGE CONSTRUCTION

Each output stage is built on a separate, electrically isolated, forced-air heat sink. Twenty NPN output transistors are directly mounted to each sink. Lower junction temperature for the output transistors is provided by this mode of operation.

The twenty output transistors are driven by two NPN bipolar transistors, each driving ten of the outputs. The output transistors are divided with ten to one side of the heat sink and ten to the other side. The driving transistors are located on the opposing sides of the heat sink. This cross-coupled orientation is used to provide thermal degeneracy on a side-to-side basis.

The entire output sink is isolated from chassis. Two of the fasteners at the middle of the heat sink are used to connect the high-current signals to the sink. The fasteners at the ends of the sinks are provided for mechanical support.

LOW SIDE ERROR AMPLIFIER

The bridge is balanced by the low side error amplifier which drives the two output stages on the low side of the bridge output. The low side error amplifier drives the low side output stages such that the feedback signal through RFB4 and RFB5 produces the same current that is produced by the input signal through RFB3 from the high side output.

PROTECTION

The output transistors are protected by simulation methods. An analog of a worst case junction temperature is computed by taking the product of the output semiconductor current and voltage and applying this stimulus to a thermal impedance analog of a worst case output device. The heat sink actual temperature is added to the result in an absolute temperature model of the junction temperature.

The low side of the bridge is sampled for voltage, current and temperature because the low side of the bridge is common to analog ground. The high side of the bridge is constrained by the bridge balance amplifier to have the same dissipation as the low side. The low side PNP output stage conducts simultaneously with the high side NPN stage to produce a positive output current.

2- GRADIENT POWER MODULE (GPM, 8651) (continued)

HEAT SINK TEMPERATURE SENSING

Integrated circuit temperature sensors are used on the low side of the bridge stages to provide information to the protection circuitry. The output of each of these sensors is a current proportional to the absolute temperature. Since the bridge is balanced in actual operation, the temperature of the NPN high side of the bridge should be essentially the same as the low side PNP output stage.

Overtemperature in the output heat sinks is prevented by bimetal switches mounted on the high side of output stage heat sinks.

FAULT

Should a failure occur that causes the output stages to conduct a large common mode current for more than a few microseconds, the amplifier will be disabled by the fault detection circuitry. In normal operation only one high side output stage and one low side output stage are conducting current at a time. If an event such as a shorted output transistor causes current to conduct simultaneously through both high side or both low side output stages, an SCR will latch the amplifier into disabled condition by removing power to the Vcc supply. The only way to clear this condition is to cycle the secondary control power supply.

2- GRADIENT POWER MODULE (GPM, 8651) (continued)

TURN ON DELAY AND STANDBY

A resistor and capacitor timing circuit form the heart of the turn on delay and standby circuit. When the unit is first powered, the capacitor is discharged and must be charged by current through a resistor. When the potential across the capacitor exceeds the ground potential on the hysteresis feedback of a comparitor, the comparitor changes states an enables the Vcc supply.

The capacitor may be discharged by six other conditions in the system.

Long Overload -- For longer than 35 milliseconds the output waveform did not match the input waveform. The power module was latched into standby. If system recovery is unsuccessful, the circuit breaker must be cycled (turned off and back on) to reset the power module.

Transistor Overtemp -- The output transistor junctions were determined to be too hot. Current in the output stages was reduced until the temperature is reduced.

Shelf Overtemp -- The HI-side output heat sinks overheated. The power module was placed into standby until the temperature is reduced.

PPBM Error -- The Poly Phase Buck Module overheated or a voltage error occurred. The power module was placed into standby until the condition is corrected. The signal also indicates a faulty free-wheeling diode. If this is the error, the power module was latched into standby, and the circuit breaker must be cycled (turned off and back on) to reset the power module.

Transistor Fault -- A short circuit was detected in the output stage transistors. The power module was latched into standby. If system recovery is unsuccessful, the circuit breaker must be cycled (turned off and back on) to reset the power module.

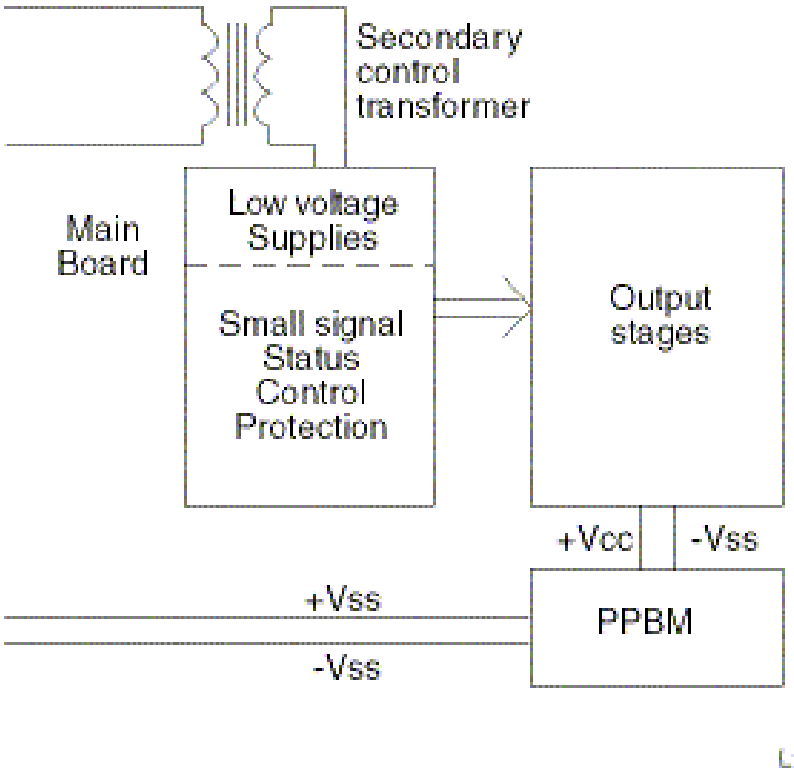
Standby Command -- The GIP can force the amplifier into a standby condition.

2- GRADIENT POWER MODULE (GPM, 8651) (continued)

POWER DISTRIBUTION

The 8651 requires two types of power supplies. Low voltage supplies are constructed on the main board and the poly phase buck module, which is a high voltage, high energy supply. See Illustration 2-3.

Small signal, control and status circuits are supplied from internal supplies powered by 208 volts AC. The ac power is supplied through a three terminal ac socket on the back of the 8651.



POWER DISTRIBUTION
ILLUSTRATION 2-3

POLY PHASE BUCK MODULE

The Poly Phase Buck Module (PPBM) is a switching power supply that tracks the output signal required to power the linear, bridged power amplifier.

2- GRADIENT POWER MODULE (GPM, 8651) (continued)

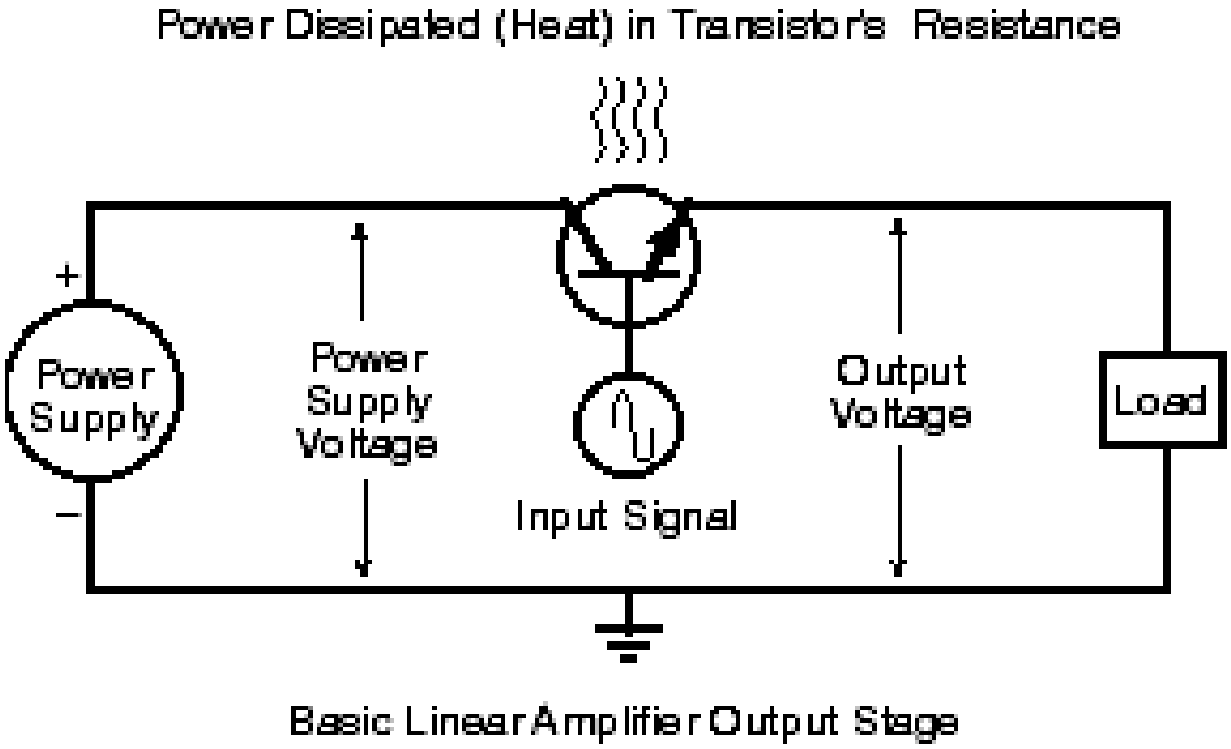


ILLUSTRATION 2-4

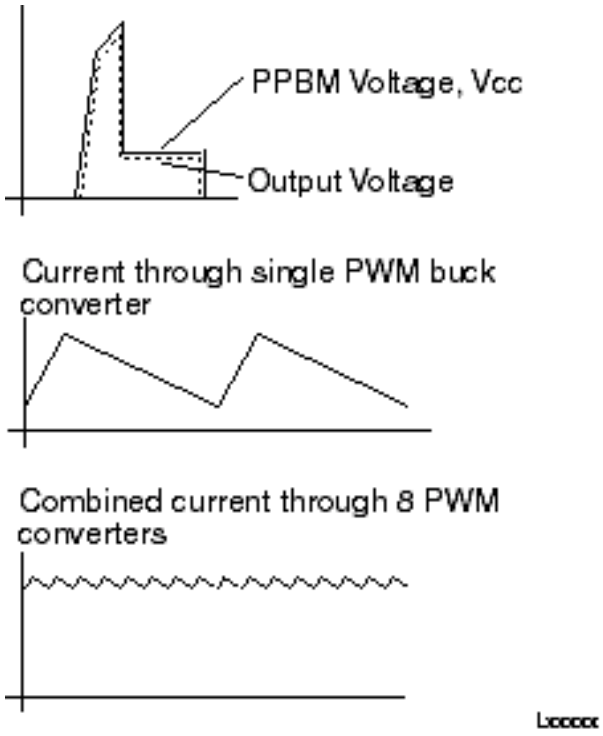
POWER DISSIPATED

In a linear amplifier the output devices act as series regulators. The devices dissipate the power difference between what is available from the power supply and what is demanded by the load as diagrammed in Illustration 2-4. Power dissipation is a product of voltage across and current through a component. Power dissipation over time results in energy dissipation (heat). Excess heat dissipation in semiconductors degrades product reliability and efficiency.

Thus, a design goal is to keep dissipation as low as possible in the output devices while still supporting the required load currents. Such a design results in lower energy dissipation in the output devices, improved efficiency, and higher reliability.

2- GRADIENT POWER MODULE (GPM, 8651) (continued)

The PPBM maintains voltage as low as is practical (typically 5 volts) across any conducting quadrant's output devices. The total PPBM voltage (Vcc) is slightly higher than the final output voltage of the power module. See Illustration 2-5.



PPBM VOLTAGE AND CURRENTS
ILLUSTRATION 2-5

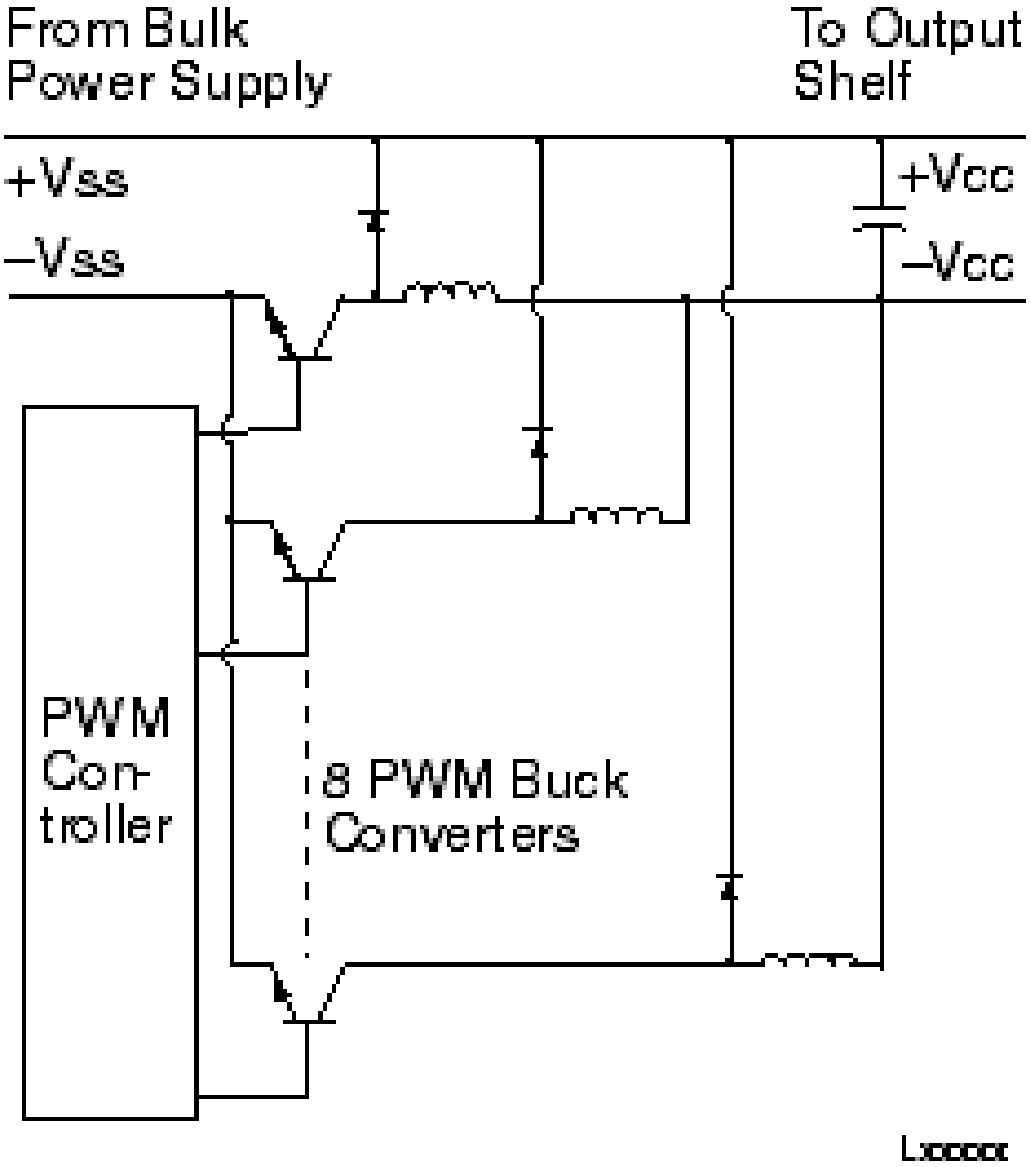
The PPBM is a switch-mode, pulse-width modulated (PWM) DC/DC regulator. The module functions as a high-power quick-response power supply. Because the needed output voltages can change rapidly (up to 40 volts per microsecond), the PPBM must also be able to respond quickly.

The PPBM consists of eight time-interleaved PWM buck converters. In each buck converter the voltage output is regulated by the length of time the series power transistors are on. The output voltage is linearly proportional to the input voltage and switch-on time. Longer pulse lengths produce higher voltages passing through to the output.

When the power transistors turn off they are protected from inductive kickback by free-wheeling diodes. The diodes bypass induced current from inductors that could damage the transistors.

2- GRADIENT POWER MODULE (GPM, 8651) (continued)

The converters are regulated by reference signals from a poly-phase PWM controller. The controller compares each converter's output with the magnitude of the amplifier's required supply voltage and current, and it modulates the switching duty cycle (time of switch-on divided by the total period) of the individual PWM converters. See Illustration 2-6.



PWM BUCK CONVERTERS
ILLUSTRATION 2-6

2- GRADIENT POWER MODULE (GPM, 8651) (continued)

The eight individual (single-phase) converters produce identical waveforms 45 degrees apart in the power conversion cycle. Each parallel 25 ampere (peak) PWM buck converter operates at 250 kHz (derived from the 2 MHz system clock by a divide-by-eight function). Combined, the buck converters produce an effective operating (ripple) frequency of 2 MHz and peak current of 250 amperes.

Each converter shares a common 200 volt dc input power source from the bulk dc supply and joins to a common pair of output terminals that lead to the bridged linear power amplifier. The PPBM output consists of the +Vcc and -Vcc voltages on the 8651 block diagram.

3- GPM POWER SUPPLY

Input power to the GPM PS shall be 208 VAC, 3 phase at 60 amps through a circuit breaker on the front of the supply. Operating input power ranges are:

Voltage Range:	208 VAC, +10%, -15%
Frequency Range:	47 to 63 Hz

The GPM Power Supply has three identical floating DC outputs that provide power to the GPM. The GPM PS provides 208 VAC, 3 phase power output for the SGD Cabinet Fan and 208 VAC for the GPM low voltage power supplies (+15V, -15V, +5V). The 208 VAC outputs pass through a 5 amp circuit breaker on the front of the supply. The key parameters of this supply are given below:

Imaging Mode:	SR77/SR120
Typical Voltage:	190V
Avg. Current:	25A

3- GPM POWER SUPPLY (continued)

All control of the GPM PS is from the GIP. Specifications for simultaneous output on each the GPM outputs is shown in the Table 3-1.

TABLE 3-1
GPM POWER SUPPLY OUTPUT

Specification	Value	Conditions
Output Voltage	190 ± 15V	Over full range of line voltage and output current. Minimum current is > 200ma draw on each output.
Output Current (average)	60A (1 output only) 30A (3 outputs simultaneous)	Continuous
Output Current (peak)	120A (1 output only) 50A (3 outputs simultaneous) 120A (3 outputs simultaneous)	t < 1.0 sec. t < 1.0 sec. t < 12 msec.
Voltage Bandwidth	500 Hz	-3 dB
Output Ripple	2V p-p	@ average output of 25A

3- GPM POWER SUPPLY (continued)

STATUS INDICATORS

The GPM PS has status LED indicators for STANDBY (yellow), ENABLE (green), READY (green) and FAULT (yellow) that are visible from the outside of the chassis.

Internally there are LED indicators for OVERVOLTAGE (red), OVERTEMP (yellow), and yellow for IGBT gate driver status which indicates the IGBT is on. The Table 3-2 shows the conditions that will set errors in the GPM PS.

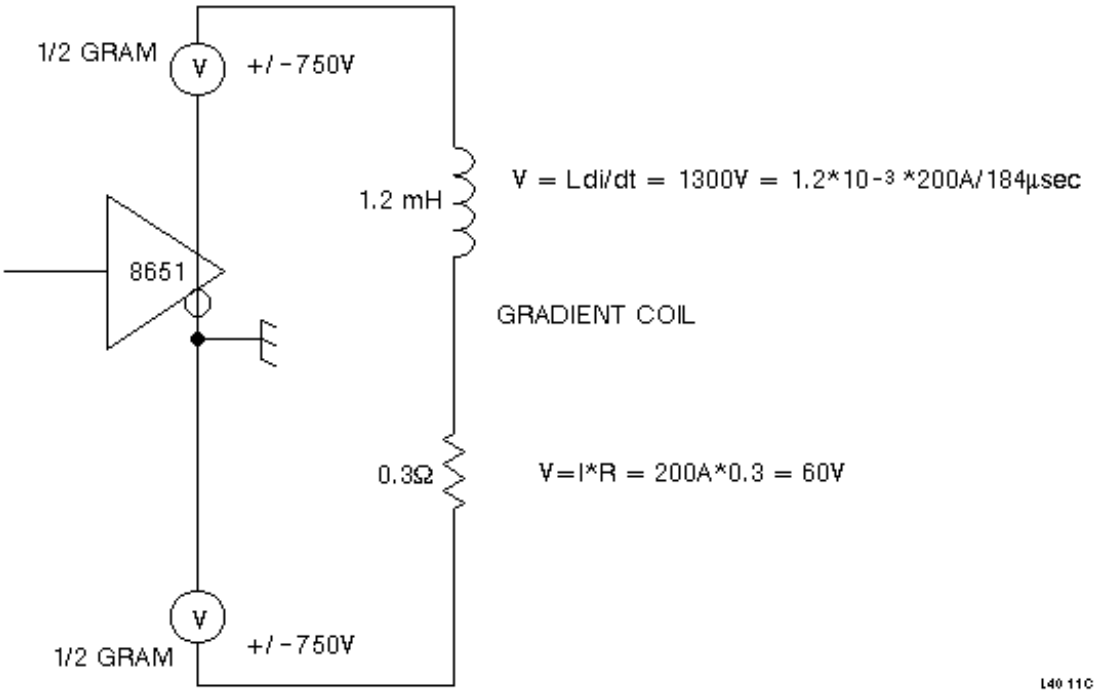
TABLE 3-2
GPM POWER SUPPLY STATUS INDICATORS

Error Status	Status Signal	Condition	How Cleared
Over Voltage (rectified outputs)	PS_FAULT	V = 215 ± 5VDC	PS_ENABLE '0' > 1ms
Over Current (Xfmr primary)	PS_FAULT	I = 600 ± 50A peak	PS_ENABLE '0' > 1ms
Over Current (all Xfmr secondaries)	PS_FAULT	I = 250 ± 25A peak	PS_ENABLE '0' > 1ms
Heatsink Overtemp	PS_FAULT	T = 70 ± 5 C	PS_ENABLE '0' > 1ms

4- MINIGRAM

The miniGRAM is the name that captures the concept of a Gradient Ramp Accelerator Module (GRAM) in a smaller designed package. The function of a GRAM in the gradient driver system is to apply high voltage to the gradient coil during a ramp, thereby reducing ramp time significantly. When the ramp reaches a plateau, the GRAM ceases to apply voltage, and the gradient amplifier maintains the constant current flowing through the gradient coil. On the descent from the plateau, the energy from the coil is recovered in large capacitors inside the GRAM, and is stored for the next ramp.

High-speed imaging requires a much faster ramp speed and greater gradient strength. The GRAM provides the additional voltage required for the faster ramps, and for a new generation of linear amplifiers. The 8651 Gradient Power Module is designed to provide the 2.2 G/cm required for some high-speed imaging techniques. The GRAM can be thought of as a programmable voltage source, or amplifier, connected in series with the 8651 linear amplifiers. Since it is independently controllable, it becomes possible to partition the voltages between the amplifiers such that the 8651 provide only the I*R drop of the gradient coil while the GRAM is programmed to provide the Ldi/dt voltage required for the rate of rise of current requested by the PSD. Illustration 4-1 shows a simplified schematic of the GRAM gradient system operating at the Signa Horizon EchoSpeed hardware configuration.



GRAM SYSTEM SIMPLE SCHEMATIC
ILLLUSTRATION 4-1

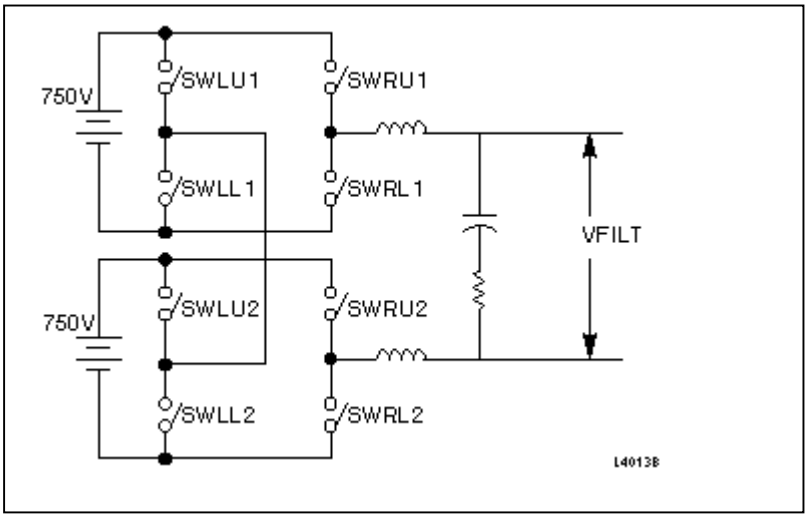
4- MINIGRAM (continued)

The GRAM assembly is part of a three-axis, high-powered gradient amplifier system for a magnetic resonance imager. Each axis consists of a linear amplifier circuit in the 8651 connected in series with a GRAM, and one axis of a gradient coil. The linear amplifier and the GRAM are each separately controllable, series-connected voltage sources that are programmed to supply the IR and eddy current losses, and Ldi/dt energy required by the gradient coil. The linear amplifier circuits are active at all times. They supply the voltage corresponding to the I*R drop in the coil resistance, and whatever voltage is required for eddy current compensation. The GRAM is active during current ramps, and supplies the Ldi/dt voltage required to force the commanded rate of change of gradient coil current. During the flattops or plateaus of trapezoidal gradient current, Ldi/dt is zero and the GRAM operates in the freewheel mode, passing current on to the gradient coil without adding voltage to it.

The miniGRAM is capable of performance at 1400V and 250A.

SWITCHING AMPLIFIER FUNCTION

Each of the 750V voltage sources shown in Illustration 4-1 is actually a switching amplifier made up of two full bridge inverters connected in series, and an LRC output filter shown schematically in Illustration 4-2. The operation of each full bridge inverter can be understood by representing each IGBT as a single-pole mechanical switch with four switches connected into a full bridge circuit with a 750V battery feeding the dc bus. The inverter is capable of producing +750V and –750V, or zero volts at its output by turning the proper switches on and off. For instance, if SWRU1 and SWLL1 are closed, 750 volts is connected to its output at the midpoints of the two inverter legs. Closing SWLU1 and SWRU1 short circuits the two midpoints together producing zero volts, and closing SWLU1 and SWRL1 produces –750 volts. A second identical inverter is connected in series with the first inverter and this combination can produce five voltage states: +1500V, +750V, 0V, –750V, and –1500V.



GRAM LRC OUTPUT FILTER MODEL
ILLUSTRATION 4-2

5- GRAM POWER SUPPLY

Input power to the GRAM Power Supply shall be 208 VAC, 3 phase at 60 amps through a circuit breaker on the front of the supply. Operating input power ranges are:

Voltage Range: 208 VAC, +10%, -15%
Frequency Range: 47 to 63 Hz

The GRAM PS has six identical floating DC outputs that supply power to the X, Y, and Z miniGRAM's. The outputs can operate at 2 voltage levels depending upon the type of gradient strength SR77 or SR120 operation.

Mode	Voltage (Typical)	Current (Average)
SR77	510V	4.8A
SR120	750V	3.3A

All control of the GRAM PS is from the GIP.

STATUS INDICATORS

The GRAM PS has status LED indicators for STANDBY (yellow), ENABLE (green), READY (green) and FAULT (yellow) that are visible from the outside of the chassis.

Internally there are LED indicators for OVERVOLTAGE (red), OVERTEMP (yellow), and yellow for IGBT gate driver status which indicates the IGBT is on. The Table 5-1 shows the conditions that will set errors in the GRAM PS.

TABLE 5-1
GRAM POWER SUPPLY STATUS INDICATORS

Error Status	Status Signal	Condition	How Cleared
Over Voltage (rectified outputs)	PS_FAULT	V = 850 ± 20VDC	PS_ENABLE '0' > 1ms
Over Current (Xfmr primary)	PS_FAULT	I = 250 ± 50A peak	PS_ENABLE '0' > 1ms
Over Current (all Xfmr secondaries)	PS_FAULT	I = 25 ± 5A peak	PS_ENABLE '0' > 1ms
Heatsink Overtemp	PS_FAULT	T = 70 ± 5 C	PS_ENABLE '0' > 1ms

REVISION HISTORY

REV	DATE	AUTHOR	PRIMARY REASONS FOR CHANGE
0	Oct 3, 1997	J. Wolak	Initial version for SGD production introduction.
1	October 13, 1999	K. Keshena	Changed to use proprietary header.