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Description - This document relates to Signa 8x systems with ACGD Gradient Cabinets. This material covers the various power-up tests that are run when the system is booted up.

1- INTRODUCTION

Gradient Driver Power-up Tests are contained in both Gradient Processor (GP) boot code and application code. The Power-up Tests are run during the boot sequence to verify the integrity of hardware components in the gradient subsystem. The boot sequence occurs every time the system is rebooted, every time there is a Reset TPS, and the first time that gradient driver tests are initiated from the touch screen. The following sections describe the basic processing involved with each test.

2- GP BOARD STATUS LEDS

The GP board has two status LEDs located on the front panel. One, labeled POWER, is always on when the GP board has power. The other, labeled HEARTBEAT, is used to provide status information to the user. During normal use, the HEARTBEAT LED flashes on and off with a period of five seconds, and a 50 percent duty cycle, to indicate that the GP is executing code. During boot code execution, the HEARTBEAT LED flashes if there is an error with the DUART or the external static RAM on the GP board.

An error with the DUART causes the HEARTBEAT LED to flash on and off with a period of one second with a fifty percent duty cycle. An error with the external static RAM causes the following HEARTBEAT LED sequence: Double flash ON, then OFF (period of 1.25 seconds). The sequence runs continually and looks like two short flashes.

Table 2-1 shows the GP Status LED flash sequences.

TABLE 2-11
GP BOARD STATUS LED FLASH SEQUENCE

LED	System Status	Flash Sequence
Heartbeat	System is OK	Single flash On/Single flash Off with a period of 5 seconds and a 50% duty cycle
Heartbeat	Boot code DUART Test Failure	Single flash On/Single flash Off, 50% duty cycle. Period of 1 second.
Heartbeat	Boot code External Static RAM Test Failure	Double flash On/Single flash Off, period of 1.25 seconds.
Heartbeat	Power-up Interrupt Test Failure	Triple flash On/Single flash Off, 50% duty cycle. Period of 1.75 seconds.
Power	+5 V Indicator	When lit, this indicates that +5 V is present. If it is not lit, +5V is not getting to the GP.

3- GP BOARD POWER-UP TESTS

3-1 Boot Code DUART Test

This test turns on the DUART internal loop back logic. Data patterns are transmitted through both channels of the DUART, and the data in the DUART register are compared to the transmitted data.

3-2 Boot Code External SRAM Test

This test writes data patterns to the SRAM address space. Data patterns then are read back and compared to the data patterns previously written. A data pattern test consists of filling all memory with a constant data value, and then reading back and verifying each memory location. This provides a simple (but not exhaustive) test of all data bits in the memory under test. The following data patterns are used to check for data bit errors and any other forms of data pattern sensitivity in memory:

0x33333333, 0x00000000, 0x55555555,
0xAAAAAAAA, 0xCCCCCCCC,
0xFFFFFFFF, 0x0F0F0F0F,
0xF0F0F0F0, 0x00FF00FF,
0xFF00FF00, 0x0000FFFF, 0xFFFF0000

An address test is performed by filling the entire GP-SRAM with an incrementing pattern, reading it back, and verifying it.

Walking zeros and ones test is an exhaustive check of GP-SRAM, it fills the memory with ones and zeros and has the zero or one slide through the entire GP-SRAM while verifying that the rest of the SRAM is unchanged.

3-3 Boot Code Flash Memory Checksum Test

This test performs the checksum test of the application code present in flash memory. Before the checksum computation is started, the header is checked to see if the device is blank. If the length field or the checksum field in the header is either all zeros or all ones, the device is blank. If the device is blank, the checksum is not computed. If it is nonblank, the checksum is computed for the application code, and is compared with the checksum field present in the header.

If power is cycled during a flash program/ erase cycle, the device is then considered blank.

The function returns 0 if successful; if it fails an error message is reported to the message log.

3-4 Power-up Interrupt Test

The Power-up Interrupt Test consists of testing the DUART Interrupt on the GP board and TIC31 Processor Interrupt. To generate a DUART interrupt, a null character is written to the debug terminal. Writing this character causes a transmit interrupt to occur from the DUART. This is detected by the TIC31 Processor.

If the interrupt is detected by the TIC31 Processor, the Power-up Interrupt Test is successful. If the TIC31 Processor times out after two milliseconds, and does not receive the interrupt, the Power-up Test is unsuccessful.

A failure of the Power-up Interrupt Test is the same as a failure of the GP FRU. The MDS Link will not be able to communicate with the GP board without interrupts functioning.

3-5 Power-up Register Test

The Power-up Register Test checks several registers on the GP Board.

At the start of the register test, the contents of all registers used during the test are saved. Likewise, these registers are restored at the conclusion of the test.

The register test begins with a rigorous pattern test. Each register is tested with all possible patterns in a counting sequence: 0000, 0001, ... 1111.

Because some registers on each board have bits that are read only, only read/write registers are tested. Bits that are read only or should not be altered, are not changed via this test.

Errors discovered through this test are logged to the message log. If any error is found, the Power-up Tests abort and the application code does not go to Ready.

REVISION HISTORY

REV	DATE	AUTHOR	PRIMARY REASONS FOR CHANGE
A	Sept. 18, 2000	K. Keshena	Preliminary release.
0	Oct. 20, 2000	K. Keshena	Initial Release.