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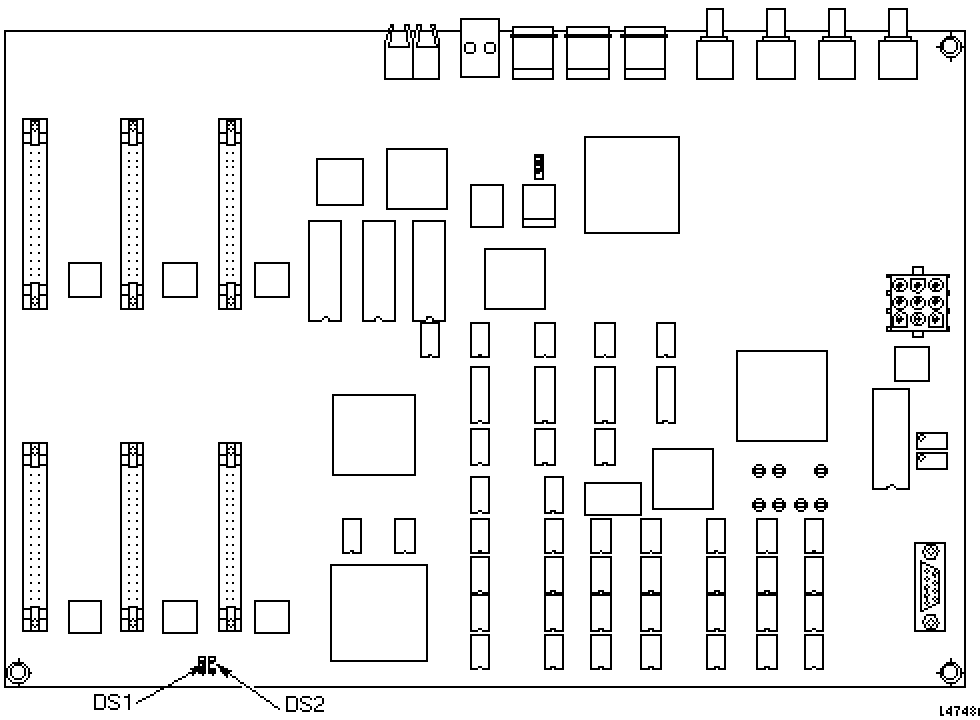
Description - This material covers the various power-up tests that are run on the 8645/GRAM hardware when the system is booted up.

1- INTRODUCTION

Gradient Driver Power-up Tests are contained in both GAP boot code and application code. The Power-up Tests are run during the boot sequence to verify the integrity of hardware components in the Gradient subsystem. The boot sequence occurs every time the system is rebooted, every time there is a Reset TPS, and every time Gradient Driver Tests are initiated. The following sections describe the basic processing involved with each test.

2- GAP BOARD STATUS LEDS

The GAP Board has two status LEDs (see Illustration L4748A). One (DS1) is always on when the GAP Board has power. The other (DS2) provides status information.



GAP BOARD STATUS LEDS
ILLUSTRATION L4748A

During normal use, LED DS2 flashes on and off with a period of 5 seconds, and a 50 percent duty cycle, to indicate that the GAP is executing code.

During boot code execution, the LED flashes if there is an error with the DUART, or the external static RAM on the GAP Board.

An error with the DUART causes the LED to flash on and off with a period of one second with a fifty percent duty cycle.

An error with the external static RAM causes it to flash on for one quarter of a second, flash off for one quarter of a second, flash on for a quarter of a second, and then flash off for one half of a second. The sequence runs continually and looks like two short flashes.

Table 1 shows the GAP Status LED flash sequences.

TABLE 1
GAP BOARD STATUS LED FLASH SEQUENCES

LED name	State	Flash Sequence
DS2 (Heartbeat LED)	System is OK	Single flash On/Single flash Off with a period of 5 seconds and a 50% duty cycle.
DS2 (Heartbeat LED)	Boot code DUART Test failure	Single flash On/Single flash Off, 50% duty cycle.
DS2 (Heartbeat LED)	Boot code External Static RAM Test Failure	Double flash On/Single flash Off, 50% duty cycle.
DS2 (Heartbeat LED)	Power-up Interrupt Test Failure	Triple flash On/Single flash Off, 50% duty cycle.
DS1	+5 V Indicator	When lit, this indicates that +5 V is present. If it is not lit, +5V is not getting to the GAP.

3- GAP BOARD POWER-UP TESTS

3-1 Boot Code DUART Test

This test turns on the DUART internal loop back logic. Data patterns are transmitted through both channels of the DUART, and the data in the DUART register are compared to the transmitted data.

3-2 Boot Code External SRAM Test

This test writes data patterns to the SRAM address space. Data patterns are then read back and compared to the data patterns previously written. A data pattern test consists of filling all memory with a constant data value, and then reading back and verifying each memory location. This provides a simple (but not exhaustive) test of all data bits in the memory under test. The following data patterns are used to check for data bit errors and any other forms of data pattern sensitivity in memory:

0x33333333, 0x00000000, 0x55555555,
0xAAAAAAAA, 0xCCCCCCCC,
0xFFFFFFFF, 0x0F0F0F0F,
0xF0F0F0F0, 0x00FF00FF,
0xFF00FF00, 0x0000FFFF, 0xFFFF0000

An address test is performed by filling the entire GAP-SRAM with an incrementing pattern, reading it back, and verifying it.

The walking zeros and ones test is a check of GAP-SRAM. It fills the memory with ones and zeros and has each zero or one slide through the entire GAP-SRAM while verifying that the rest of the SRAM is unchanged.

3-3 Boot Code Flash Memory Checksum Test

This test performs the checksum test of the application code present in flash memory. Before the checksum computation is started, the header is checked to see if the device is blank. If the length field or the checksum field in the header is either all zeros or all ones, the device is blank. If the device is blank, the checksum is not computed. If it is not blank, the checksum is computed for the application code, and is compared with the checksum field present in the header.

If power is cycled during a flash program/-erase cycle, the device is then considered blank.

The function returns 0 if successful; if it fails, it returns one of two different error codes, depending on the type of failure. It returns EM_GAP_FLASH_BLANK if the device is blank, and EM_GAP_FLASH_ CHKSUM_FAIL if it fails in the checksum test. Any error message is reported to the message log.

3-4 Power-up Interrupt Test

The Power-up Interrupt Test consists of testing the DUART Interrupt on the GAP Board, along with the Programmable Interrupt Controller (PIC), and TIC31 Processor Interrupt. To generate a DUART interrupt, a null character is written to the debug terminal. Writing this character causes a transmit interrupt to occur from the DUART. This is detected by the PIC and, finally, the TIC31 Processor.

If the interrupt is detected by the TIC31 Processor, the Power-up Interrupt Test is successful. If the TIC31 Processor times out after two milliseconds, and does not receive the interrupt, the Power-up Test is unsuccessful.

A failure of the Power-up Interrupt Test is the same as a failure of the GAP FRU. The MDS Link will not be able to communicate with the GAP board without interrupts functioning.

3-5 Power-up Register Test

The Power-up Register Test checks all MIF, ASM, GRAM, and GASM boards existing in the Gradient subsystem. Since application code is not yet initialized, Power-up Tests have no knowledge of the configuration selected in the `MRconfig.cfg` file. Therefore, Power-up Tests simply sense the hardware present and test what is there.

At the start of the Register Test, the contents of all registers used during the test are saved. Likewise, these registers are restored at the conclusion of the test.

The Register Test begins with a rigorous pattern test of one register on each board. Each four-bit register is tested with all sixteen possible patterns in a counting sequence: 0000, 0001, ... 1111. Table 2 defines the registers exercised in this test.

TABLE 2
POWER-UP REGISTER TEST BOARD PATTERN REGISTERS

Board	Pattern register
MIF	If board revision < 2: MIF_REG_FULL_SCALE (register 0x6) If board revision ≥ 2: MIF_REG_DIAG (register 0xD)
ASM	ASM_GASM_REG_OFFSET_3_0 (register 0x13)
GRAM	GRAM_REG_DIAG (register 0xD)
GASM	ASM_GASM_REG_OFFSET_3_0 (register 0x13)

All boards and all axes present are tested with the patterns. If after collecting data on all boards and axes, it is discovered that power may be off to the board(s), the Register Test is halted and an error is logged. Otherwise, if an overall conclusion (such as power off) cannot be made, an error is logged based on the number of errors in the pattern portion of the Register Test, and the test continues with the register addressing portion.

Following the pattern register test, a test is made to uncover any register addressing errors. Three registers on each board are tested by writing two unique patterns to each and verifying the registers were written. Table 3 defines the registers exercised in this test.

TABLE 3
POWER-UP REGISTER TEST ADDRESSING TEST BOARD REGISTERS

Board	Addressing Test registers
MIF (if board revision <2)	MIF_REG_FULL_SCALE (register 0x6) MIF_REG_ANALOG_VIN (register 0x7) MIF_REG_MASK (register 0x8)
MIF (If board revision ≥2)	MIF_REG_FULL_SCALE (register 0x6) MIF_REG_MASK (register 0x8) MIF_REG_DIAG (register 0xD)
ASM	MIF_REG_FULL_SCALE (register 0x6) MIF_REG_MASK (register 0x8) MIF_REG_DIAG (register 0xD)
GRAM	GRAM_REG_FREEWHEEL (register 0x6) GRAM_REG_GRAM_MODE (register 0x7) GRAM_REG_DIAG (register 0xD)
GASM	ASM_GASM_REG_OFFSET_3_0 (register 0x13) ASM_GASM_REG_OFFSET_7_4 (register 0x14) ASM_GASM_REG_GAIN_11_8 (register 0x18)

Because some registers on each board have bits that are *read only*, masks are used when executing the addressing test. Bits that are *read only*, or should not be altered, are not changed via this test.

Errors discovered through this test are logged to the message log. If any error is found in either the pattern test or the addressing test, the Power-up Tests abort and the application code does not go to Ready.

REVISION HISTORY

REV	DATE	AUTHOR	PRIMARY REASONS FOR CHANGE
0	May 22, 1998	J. Saperstein	Initial conversion from Toolbook to Word