TABLE OF CONTENTS

Description - This material, covering Gradient Driver subsystem diagnostics, applies only to Signa Horizon systems with 8645/GRAM hardware.

1- GRADIENT DRIVER TESTS

1-1 Introduction

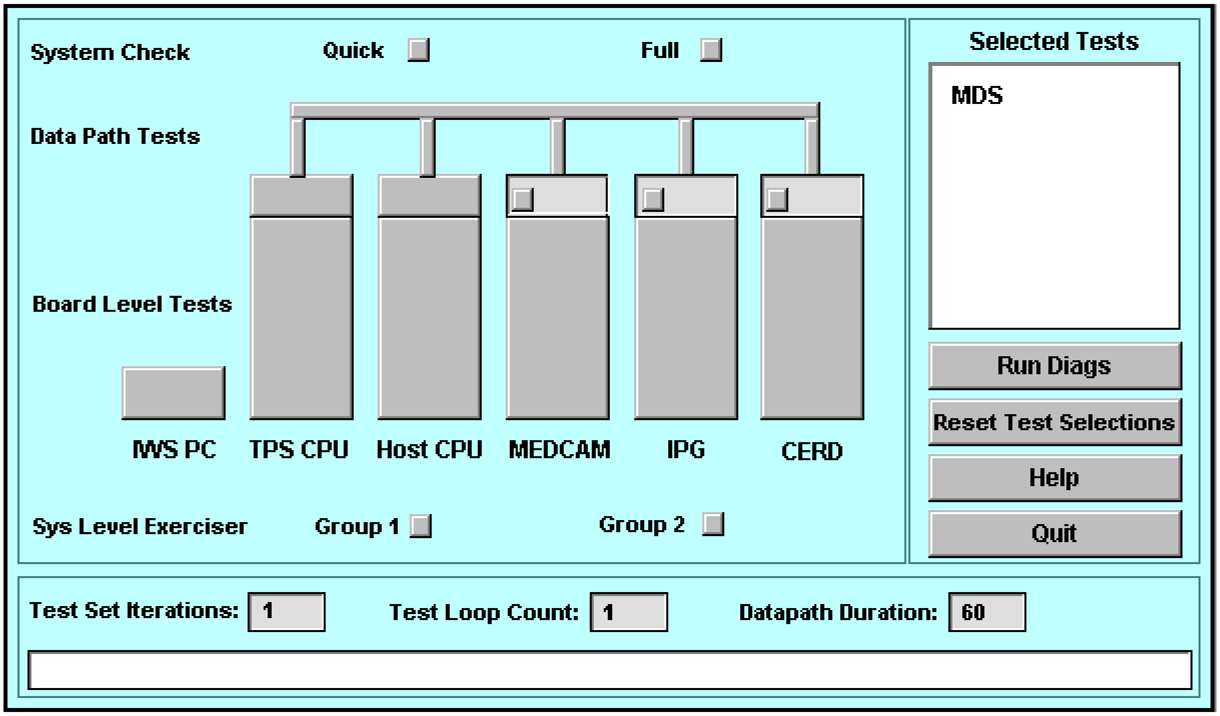
Gradient Driver Tests are a new way of testing the Gradient Driver subsystem. The tests look like diagnostics that are invoked on the screen at the operator work space. They are more than that, however; they are a hybrid digital and analog diagnostic test. This group of tests exercise and test the entire Gradient Driver subsystem with the three non-proprietary Power-up Tests, and the proprietary Static and Dynamic Tests.

The Gradient Driver Tests use the GASM (GRAM Analog Service Module), if present, and the ASM (Analog Service Module) to look at digital and analog signals within the Gradient Driver subsystem.

The Gradient Driver Tests are designed to isolate a problem in a FRU, or group of FRUs. The tests are easy to invoke, and they exercise the Gradient Driver subsystem. Errors are reported to the error log with extended information in the Extended Error Log (EEL). For more information on the EEL, see procedure for Gradient Driver Extended Error Log Overview.

2- RUNNING GRADIENT DRIVER TESTS

1. Select the Diags Main Menu from the **[Diagnostics]** menu on the Service Desktop, then click **[Start]**.
2. Wait for the Diagnostics Main Menu to appear, as shown in Illustration 1-1.



MDS

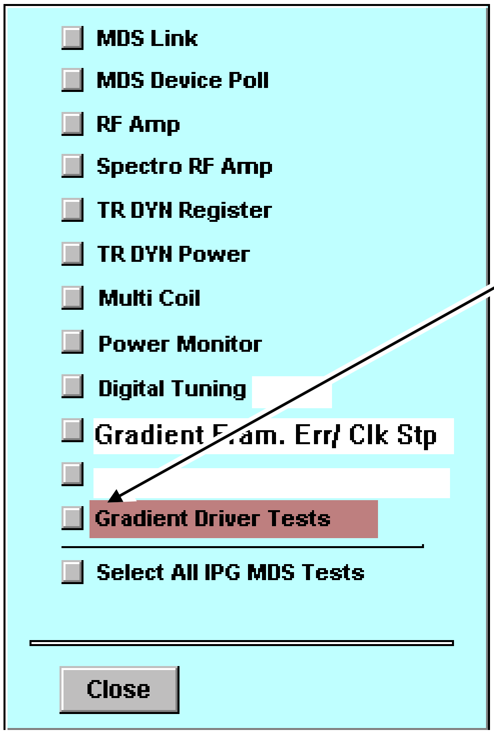
Test Set Iterations: 1

Test Loop Count: 1

Datapath Duration: 60

DIAGNOSTICS MAIN MENU SCREEN
ILLUSTRATION 1-1

3. Select iteration count: **[1]** (default), **[5]**, or **[Cont]** (continuous).
4. Click on **IPG**, then **[MDS...]**.



TEST SELECTION SCREEN
ILLUSTRATION 1-2

5. Select **[Grad Driver Tests]**. Then click on **[Close]**, then **[Close]** again. See Illustration 1-2.

6. Click on **[Run Diags]**. A *Results* window will appear along with a status message indicating the TPS is resetting. Once the TPS reset is complete, the selected diagnostic test will automatically commence. To halt the test, click on **[Stop Diags]**.

3- POWER-UP TESTS

Power-up Tests examine power supplies, digital registers, cable connections, and interconnects. They run each time the system is brought up to the applications level, each time the TPS is reset, and the first time the Gradient Driver Tests are invoked from the Diagnostic menu on the Service Desktop.

When the IPG/SPI code is loaded the first time, Diagnostics are executed, which in turn does a TPS Reset. All subsequent Run Diags sessions do not run Power-up Tests.

When Gradient Driver Tests are run the first time, the TPS is reset. That reset invokes the Power-up Tests. After that, the ASM/GASM Local Voltage Check, Static Tests, and Dynamic Tests occur. These are explained next.

For a complete description of the Power-up Tests, see the procedure for Gradient Driver Power-up Diags.

4- ASM/GASM LOCAL VOLTAGE CHECK

This test performs a basic check of constant voltages on the ASM and GASM Boards present in the system. Table 1 defines the signals that are tested.

TABLE 1
LOCAL VOLTAGE CHECK SIGNALS TESTED

Analog Service Module	GRAM Analog Service Module
Analog Ground	Analog Ground
5V Digital Reference	VOC Reference
15V Reference	15V Reference
5V Reference	5V Reference
1.235V	1.235V

Each signal is checked on each axis to be within the defined run time monitoring range. If a signal is out of range, an error is logged in the Application Error Log and the Diags Error Log. Consistent errors, such as all signals reading 0 volts on a board, are logged as a probable power off or bad cable connection.

5- STATIC TESTS

These diagnostics test for three possible hardware configurations and operating modes. They exercise the Gradient Driver subsystem in the most comprehensive manner, and also in the same modes used in product. Together with the Power-up Tests, these Static Tests establish confidence in the following areas of the subsystem.

- Digital portions of the GAP Board
- Digital Portions of the MIFs, ASMs for all products
- Digital portions of the GRAMs and GASMs for Signa Horizon HiSpeed and Signa Horizon EchoSpeed
- The entire MDS Link
- The analog signals on the Power Modules
- The analog signals on the GRAMs
- The entire analog gradient driver feedback loop

Prior to starting the Static Tests, a comparison is made between the hardware configuration specified in the `MRconfig.cfg` file, and the actual hardware sensed by the GAP Board. If the two do not match, the Gradient Driver Tests are aborted. It is critical that the MR configuration file and the hardware present match exactly for these tests to operate. If they do not match, Gradient Driver Tests are not executed for any axis.

5-1 Static Fault Checking

Prior to beginning the Static Tests, all fault registers on the MIF and GRAM are checked. Table 2 lists the signals tested.

TABLE 2
STATIC TEST SIGNALS TESTED

MIF	GRAM
Shelf Overtemp – High Power Module	I-Amp (Amplifier Overcurrent)
Shelf Overtemp – Low Power Module	I-Amp (Output Overcurrent)
Transformer Overtemp – High Power Module	Shoot Through (ST)
Transistor Fault – High Power Module	DC Overcurrent
Transistor Fault – Low Power Module	Over Voltage
PPBM Fault – High Power Module	Under Voltage
PPBM Fault – Low Power Module	Wiring Fault
Die Overtemp Nolatch – High Power Module	IGBT Overtemperature
Die Overtemp Nolatch – Low Power Module	Current Distorted
- -	Avg_OC (Average current above limit)
- -	Ground Loss

If any of the faults (in Table 2) are set, an error is logged, and NO Dynamic Tests are performed. Always use the Extended Error Log (EEL) for additional servicing information.

Faults are also monitored during the operation of the test. If a fault occurs, an error is logged and the test is aborted on that axis.

5-2 Static Tests Modes

There are four modes in which the Static Tests run:

- Standby/Voltage Controlled Mode
- Ready/Voltage Controlled Mode
- Ready/Current Controlled Mode
- Ready/GRAM Current Controlled Mode

Each mode is run in the Standby and Ready states. Since each product configuration has different gradient hardware, the tests are a bit different.

For Signa Horizon (SR-20) the tests and hardware configurations are:

- Standby/Voltage Controlled Mode: 6 Power Modules
- Ready/Voltage Controlled Mode: 6 Power Modules
- Ready/Current Controlled Mode: 6 Power Modules

For Signa Horizon HiSpeed (SR-77) the tests and hardware configurations are:

- Standby/Voltage Controlled Mode: 3 Power Modules and 3 GRAMs

- Ready/Voltage Controlled Mode: 3 Power Modules and 3 GRAM
- Ready/Current Controlled Mode: 3 Power Modules and 3 GRAM
- Ready/GRAM Current Controlled Mode: 6 Power Modules and 3 GRAMs

For Signa Horizon EchoSpeed (SR-120) the tests and hardware configurations are:

- Standby/Voltage Controlled Mode: 6 Power Modules and 3 GRAMs
- Ready/Voltage Controlled Mode: 6 Power Modules and 3 GRAMs
- Ready/Current Controlled Mode: 6 Power Modules and 3 GRAMs
- Ready/GRAM Current Controlled Mode: 6 Power Modules and 3 GRAMs

5-3 Static Data Collection

Each Static Test consists of forcing DAC values and measuring a set of signals. All tests sequence through two passes. The first uses a small range of DAC values to catch any overcurrent conditions before damaging hardware. The second pass uses the full scale range from –200A to +200A, with steps every 10A. The only exception is the Ready/Voltage Controlled mode, which has a smaller DAC range to protect the hardware. If any signals are out of range in the first pass, an error is logged and the test is aborted.

5-4 Static Data Analysis

Throughout the Static Tests, signals are generated and data are collected. To determine the relative health of the hardware, transfer functions are calculated using the data collected to determine if those data are within range. This is the method that these tests use to predict where a problem is in the subsystem.

5-5 Static Tests Error Handling

Each axis of the Gradient Driver subsystem is tested independently. If an error occurs on one axis, the error is logged, the axis is taken to Standby, and the test on that axis aborts; however, all other axes, continue with the rest of the Static and Dynamic Tests.

5-6 Static Tests Error Reporting

Every error message that could be generated by the Static Tests has been reviewed for technical accuracy and service relevance. In all cases, if there were more information that could be added to the error message, an extended error message has been created. Use the EEL procedure for Gradient extended Error Log utility on your laptop to gain access to the extended error information.

6- DYNAMIC TESTS

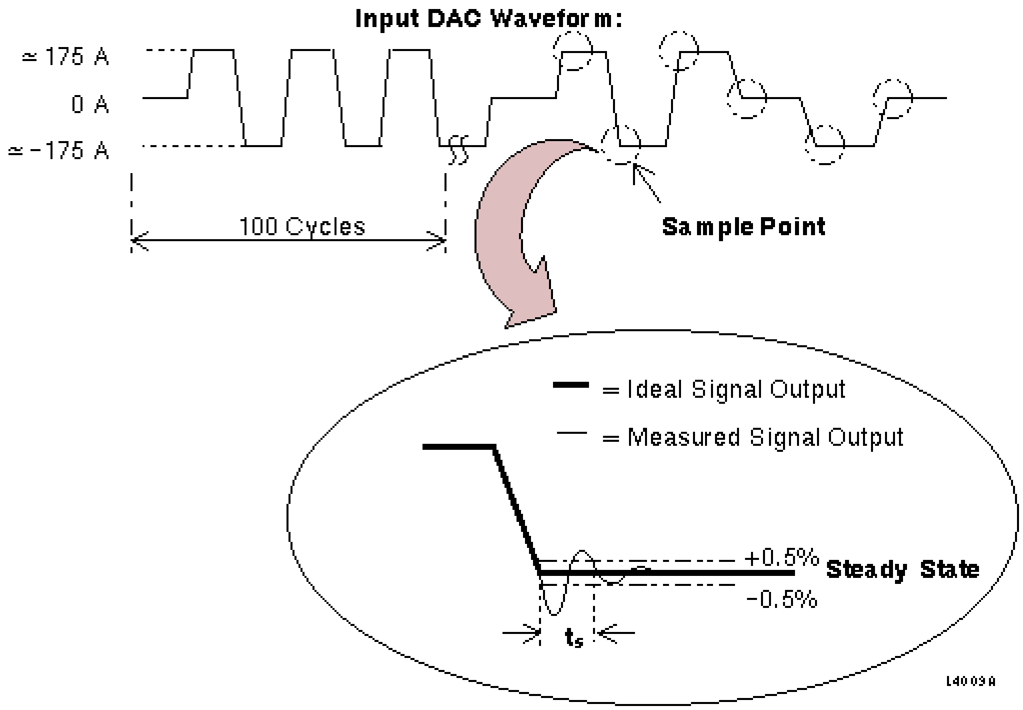
The Dynamic Tests are executed sequentially after a successful run of the Static Tests. This group of tests actually has IPG-generated waveforms. This means that voltages and currents are generated and played out using the Gradient Driver subsystem circuitry, and the epoxy-filled Gradient Coil. This digital and analog test uses a waveform that is played out to provide a unique look at analog information for diagnostic purposes.

The test that is run during the Dynamic Tests portion of the Gradient Driver Tests is called the *Settling Time Test*.

6-1 Settling Time Test

This Dynamic Test verifies that a measured 8645, or GRAM, signal settles into its steady state value within a predefined settling time. Settling time is defined as *the time required for a signal to reach and remain in a ±0.5% window of the ideal steady state voltage or current*.

Illustration L4009A shows the Settling Time Test waveforms and sample times. The upper portion of the illustration shows the overall waveform used during the test. The DAC Input is cycled through several swings of current. After loading down the system with 100 cycles, the sample phase is entered. In this phase, the DAC signal is taken from 0A to approximately 175A to approximately –175A to approximately 175A to 0A to approximately –175A to 0A, to explore each of the major transition points of the waveform. Each transition point in the illustration is indicated by a dashed circle.



SETTLING TIME TEST WAVEFORMS AND SAMPLE TIMES
ILLUSTRATION L4009A

At a transition point, the resultant output signal exhibits an overshoot and damped oscillation to its steady-state value (as shown in the exploded view in the illustration). The Settling Time Test verifies that the output signal enters the ±0.5% window within the defined settling time (t_S).

6-2 Dynamic Fault Checking

Prior to beginning the Settling Time Tests, all fault registers on the MIF and GRAM are checked. Table 3 lists the signals tested.

TABLE 3
SETTLING TIME TEST FAULT CHECKING

MIF	GRAM
Shelf Overtemp – High Power Module	I-Amp (Amplifier Overcurrent)
Shelf Overtemp – Low Power Module	I-Amp (Output Overcurrent)
Transformer Overtemp – High Power Module	Shoot Through (ST)
Transistor Fault – High Power Module	DC Overcurrent
Transistor Fault – Low Power Module	Over Voltage
PPBM Fault – High Power Module	Under Voltage
PPBM Fault – Low Power Module	Wiring Fault
Die Overtemp Nolatch – High Power Module	IGBT Overtemperature
Die Overtemp Nolatch – Low Power Module	Current Distorted
Overload	Avg_OC (Average current above limit)
- –	Ground Loss

If any of the faults (in Table 3) are set, an error is logged and no Dynamic Tests are performed. Always use the EEL for additional servicing information.

6-3 Dynamic Tests Modes

There are two modes that the Dynamic Tests run, depending on the Signa system present (i.e., whether or not you have GRAM boards).

- Current Controlled Mode
- GRAM Current Controlled Mode

6-3-1 Signa Horizon

The tests and hardware configurations are:

- Ready/Current Controlled Mode: 6 Power Modules

6-3-2 Signa Horizon EchoSpeed, and Signa Horizon HiSpeed

The tests and hardware configurations are:

- Ready/GRAM Current Controlled Mode: 3 or 6 Power Modules and 3 GRAMs

6-4 Dynamic Data Collection

The IPG generates the Input DAC Waveform for this test. At transition points, the IPG and GAP are synchronized so that the GAP begins collecting output signal samples every 32 µsec. Since the IPG has the ability to control the waveform with 4-µsec precision, the IPG actually plays out the dynamic waveform eight times, with a 4-µsec offset each cycle. The GAP, with a 32-µsec sampling ability, collects all eight offset waveforms and interleaves the collected data. This interleaving provides 4 µsec spaced signal data, and therefore, more precise collected data. Depending on the settling time, samples are collected until it is guaranteed that the output signal must be in the ±0.5% window. If the output signal is not within the window, the test fails and an error is logged.

6-5 Dynamic Data Analysis

Throughout the Dynamic Tests, signals are generated, and data are collected. This is how these tests predict where a problem is in the subsystem. The entire process is automated, and is performed within the Dynamic Tests software. Service strategies are then determined and reported in the error log and the EEL.

6-6 Dynamic Tests Error Reporting

Every error message that could be generated by the Static Tests has been reviewed for technical accuracy and service relevance. In all cases, if there were more information that could be added to the error message, an extended error message is created. Use the EEL procedure for Gradient Extended Error Log utility on your laptop to gain access to the extended error information.

7- TROUBLESHOOTING TIPS

The Gradient Driver Tests depend on the MDS Link being able to communicate. They also depend on the ASM and GASM. If the ASM is not healthy, then the data that passes through the ASM Board could be incorrect. The same is true for the GASM. An easy way to ensure that these boards are healthy is to swap the ASM from the faulted axis with the ASM from an axis with no faults. If the problem moves, then the problem is with the ASM. If this is the case, then that axis can be run without an ASM as long as the MR configuration file is updated with no ASM present for that particular axis. If the problem stays on the same axis, then further troubleshooting is necessary.

REVISION HISTORY

REV	DATE	AUTHOR	PRIMARY REASONS FOR CHANGE
0	May 21, 1998	J. Saperstein	Initial conversion from Toolbook to Word format
1	Mar. 16, 1999	F. Fiore	Change section 2 based on bay validation.
2	October 13, 1999	K. Keshena	Changed to proprietary header.