ERBTEC 20KW MAGNETIC RESONANCE IMAGING AMPLIFIER MODER 86–013–0000

PROPRIETARY MANUAL 86–013–0501

REVISION HISTORY

Each page of this manual carries its own revision level located at the top right corner of the page. The revision numbering begins with Rev 1.1.

Revisions of the second numeral indicate minor changes such as spelling and wording which do not critically affect operation of the amplifier. The second–level revision of this type is numbered as Rev 1.2.

Revisions of the first numeral indicate that significant changes affecting amplifier operation have been made. The second level revision of this type is labeled as Rev 2.1.

The listing below indicates the current revision level of each page as of the date indicated for the revision of this page (i).

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CHAPTER 1 OVERVIEW OF AMPLIFIER

Section 1.1 Block Diagram

Below is a simplified block diagram depicting the modular functionality of the ERBTEC MRI amplifier. Each block is a “field replaceable” part as discussed in Chapter 6 of the 86–013–0502 *Service Manual*. Complete schematics and wiring diagrams for the entire amplifier are also located in the *Service Manua*l, Chapter 5.

The principal operational details of each of the modules depicted below are provided in Chapter 2, *Theory of Operation*.

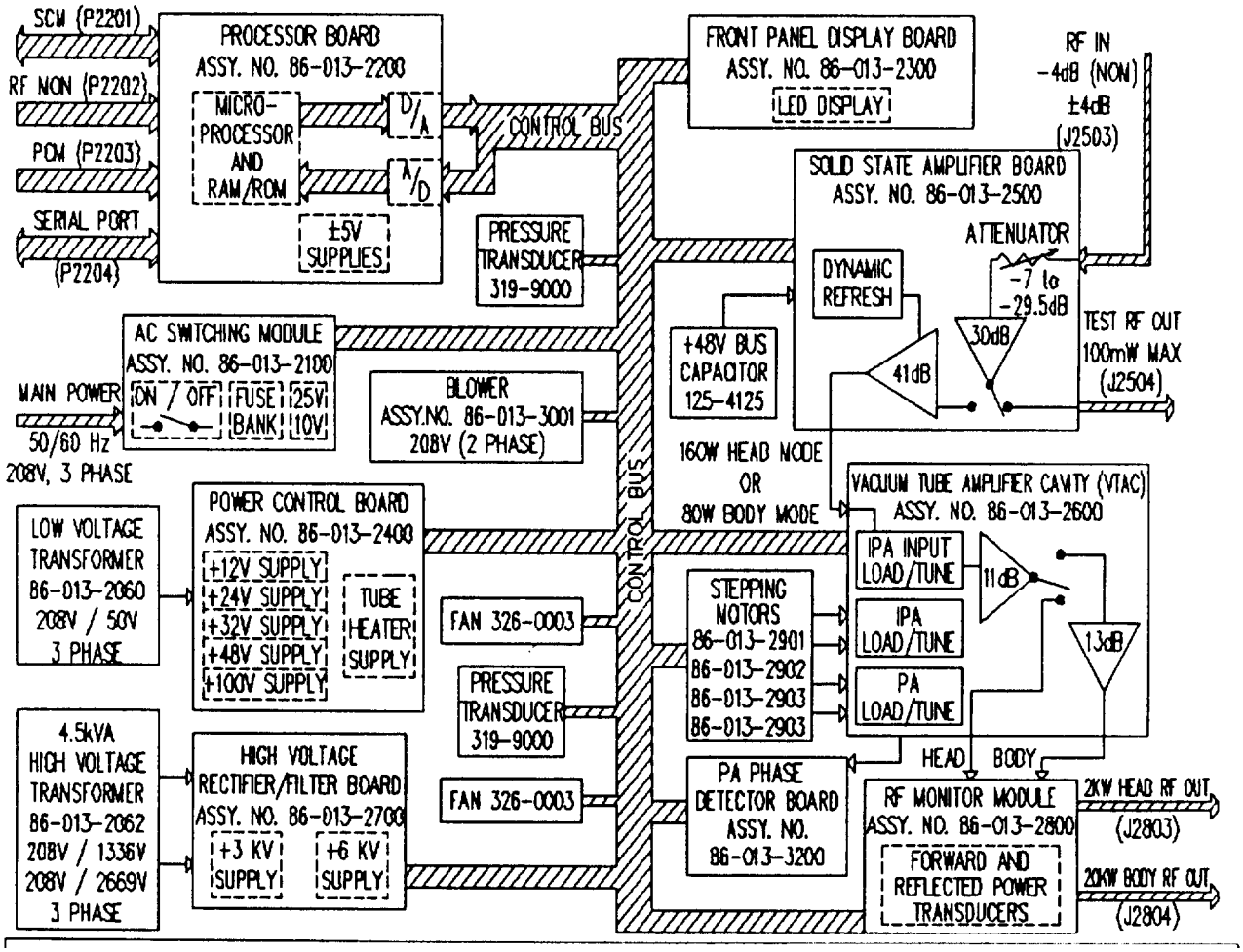

Figure 1–1 Erbtec MRI Amplifier Simplified Functional Block Diagram

Section 1.1 Block Diagram (Continued)

The diagram in Figure 1–1 is intended to provide an overall picture of the fundamental operation of the Erbtec amplifier. As can be seen, the microprocessor is the lifeline of the amplifier, extending to every block. The power supplies are located on the Power Control Board, Processor Board, and the High Voltage Rectifier/Filter Board. These modules also extend power lines throughout the amplifier. The power lines have been omitted from the diagram for clarity.

NOTE:

The terms “boards” and “modules” are often used interchangeably in this manual. See the *Service Manual*, Chapter 6 for the official title of a part, board, module, or assembly when ordering field replacements.

Section 1.2 Technical Specifications

NOTE:

Complete technical specifications for this amplifier may be found in GE MRI Specification 46–271 962.

SPECIFICATIONS:

Frequency:	Center–tuned to 63.86 MHz63.66 MHz to 64.06 MHz specification compliance band
RF input:	50 ohm impedance (VSWR < 1.5:1 over bandwidth) –30 dBm to –4 dBm (+/4 dB) range (linear operation) + 20 dBm maximum
RF Output:	50 ohm impedance Test mode: 100 milliwatts pulsed (max linear) Head mode: 2 kilowatts pulsed (max linear) Body mode: 20 kilowatts pulsed (max linear)
Max Pulsewidth:	20 milliseconds in the Head and Body modes

RF Turn–Off Conditions (Firmware selectable):

Power> 27 KW for time > 1 ms, Body mode (non–fatal fault)
Power> 3 KW for time> 1 ms, Head mode (non–fatal fault)
Power < –20dB of selected power level for time > 30 ms
VSWR > 9:1

RF Turn–Off Features:

Power out < –50 dBm within 10 microseconds of Blanking signal
Power out < 30 dBm within 100 milliseconds of Turn–off Condition

Section 1.2 Technical Specifications (Continued)

Max Phase Shift: +/–5 degrees

Noise Power (any 50 kHz band within operational bandwidth):
Noise < –1 17 dBm, Blanking on
Noise < 0 dBm, Blanking off (Unblank)

Total Harmonic Power:
Total Harmonics < –30 dBC

RF Leakage (unselected RF outputs):
Leakage < 30 dB of power at selected output

Unblank Response Time:
250 microseconds after Unblank signal start

Automatic Tuning:
Field replaceable tubes
Tuned each Standby to Operate cycle

Line Voltage:
208 VAC, +/– 10%, 47– 63 Hz, 14 amps per phase
RF Output variation < 0.15 dB per volt line voltage variation

Communication Links:
General Electric BISYCL
General Electric BICYCLE
RS–232

Interface Connectors:
P2203 PCM: 9 pin subminiature D–type male
P2202 RF MON: 9 pin subminiature D–type male
P2201 SCM: 37 pin subminiature D–type male
P2204 SERIAL: 25 pin subminiature D–type male
J2503 RF INPUT: 50 ohm coaxial type BNC female
J2504 TEST RF OUT: 50 ohm coaxial type BNC female
J2803 HEAD PORT: 50 ohm coaxial type N female
J2804 BODY PORT: 50 ohm coaxial type HN female

Section 1.3 General Amplifier Operation

The model 86–013–0000 Erbtec 20 kilowatt (KW) Magnetic Resonance Imaging (MRI) Amplifier is operated by commands issued from a controlling computer and sent to the amplifier through the SCM interface or the serial RS–232 interface. All operational connections to the MRI amplifier are made on the rear panel. Amplifier status is indicated on the front panel. The front and rear panels are shown in Figure 1–2 and Figure 1–3 respectively.

Section 1.3.1 Amplifier External Cabinet

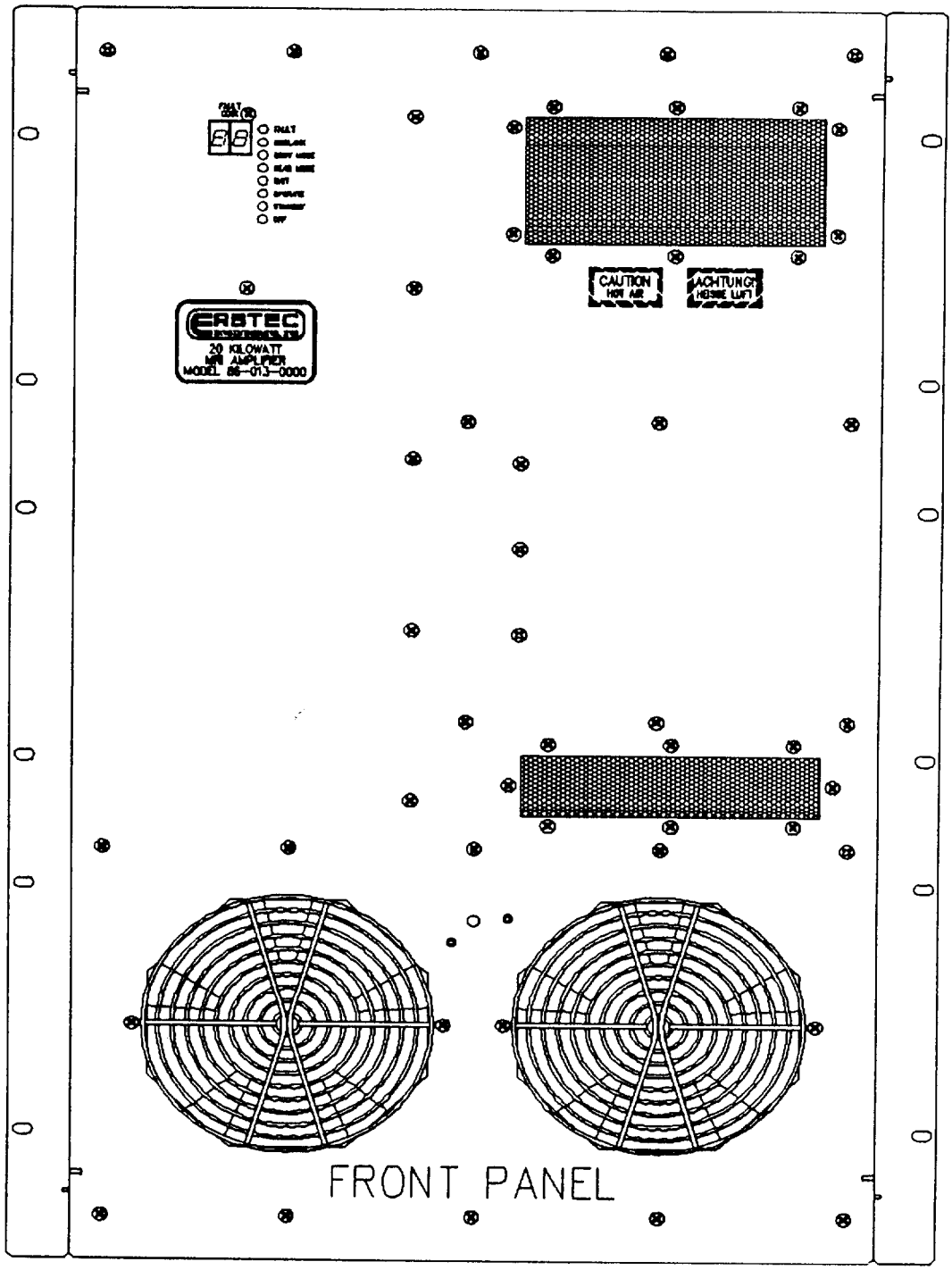

Figure 1–2 Amplifier Front Panel

Section 1.3.1 Amplifier External Cabinet (Continued)

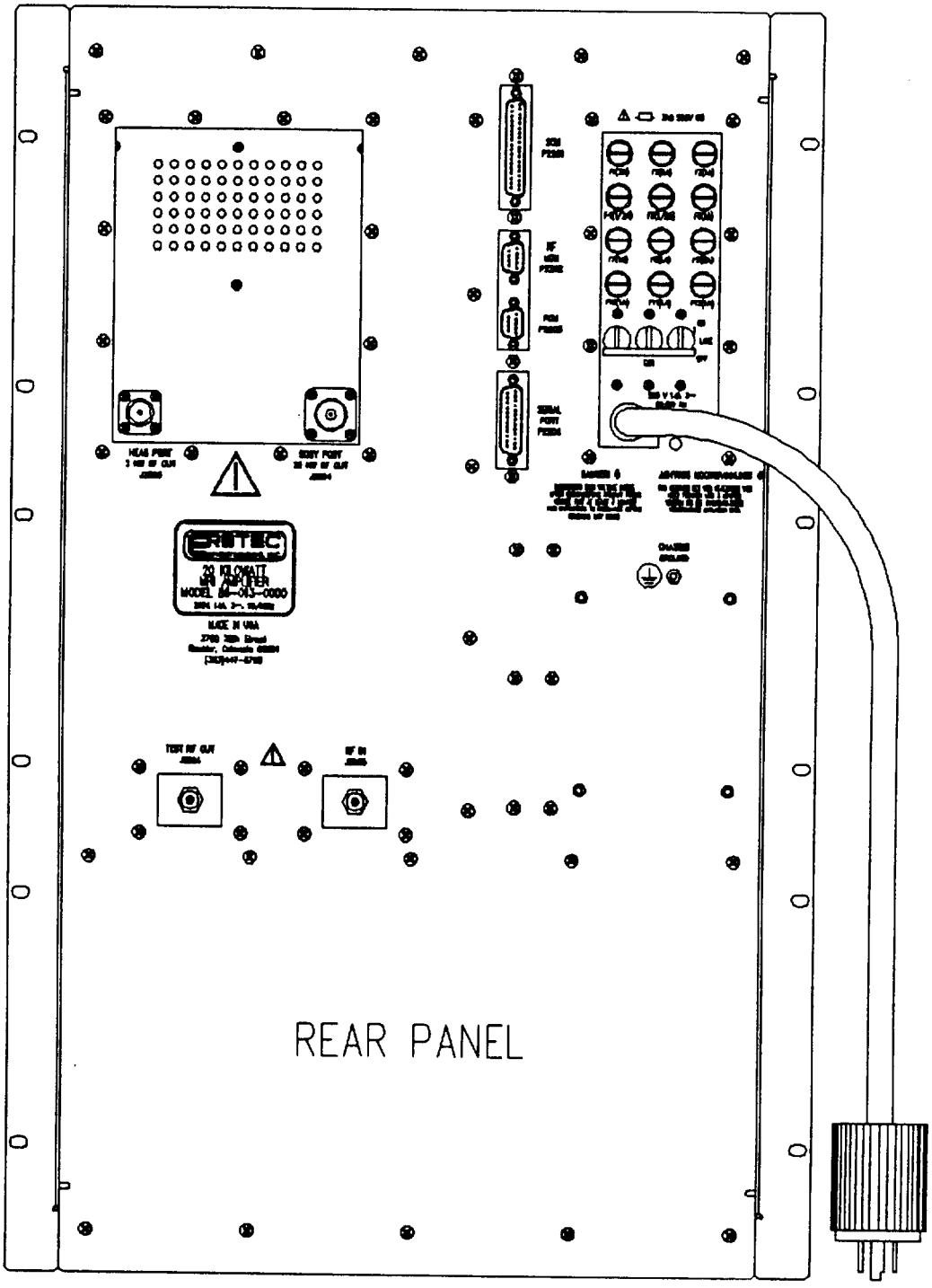

Figure 1–3 Amplifier Rear Panel

Section 1.3.1 Amplifier External Cabinet (Continued)

FRONT PANEL DESCRIPTION

LEDs: At the top left of the front panel is a display of light–emitting diodes (LEDs) and a numerical digit display labeled FAULT CODE. The purpose of each indicator is as follows:

- **OFF yellow LED** indicates the main circuit breaker CB1 on the rear panel is on, and the amplifier has not been instructed (or allowed) to proceed to a STANDBY mode.
- **STANDBY green LED** indicates the amplifier is proceeding with its self test and warm up, and will be ready to go to OPERATE when the WAIT LED is off.
- **OPERATE green LED** indicates that the amplifier is in full operational mode when the WAIT LED is off.
- **WAIT yellow LED** is on for approximately five minutes for an OFF to STANDBY cycle and a few seconds for a STANDBY to OPERATE cycle. The amplifier will not act on commands when this indicator is lit. WAIT is also lit during a shutdown procedure and briefly during mode transitions.
- **HEAD MODE green LED** indicates that the 2 KW RF output power amplification mode has been selected.
- **BODY MODE green LED** indicates that the full power 20 KW RF output mode has been selected.
- **UNBLANK yellow LED** is lit when an UNBLANK (enable output) signal is received. An UNBLANK must be received with each RF pulse for amplification to occur.
- **FAULT red LED** is lit when some internal or external irregularity is detected. The amplifier terminates the current mode of operation and goes to either STANDBY for “non–fatal” faults or OFF for “fatal” faults.
- **FAULT CODE red LED** numerical display presents a number in the range of 00–99 when an irregularity is detected. A complete listing of the fault codes is provided in Chapter 4.

The air intake fans and air exhaust vents are also located on the front panel. The fans are located at the bottom, and the air exhaust vents are located along the right side.

REAR PANEL DESCRIPTION:

LINE ON/OFF is located on the right side towards the top of the rear panel, and is labeled CB1 (circuit breaker 1) underneath the switch. The breaker functions as both the main power switch and a 250 volt, 15 amp circuit breaker to provide main power limiting protection.

Section 1.3.1 Amplifier External Cabinet (Continued)

F1–F12 is a bank of 12 fuses that provides current limiting protection for the entire amplifier. Fuse function is detailed in Chapter 4. The labeling above the fuse bank defines the type of fuses to be used; the current rating is found beside each fuse.

208 V, 14 A, 3–(phase), 50/60 Hz defines the main power to be supplied by the power cord.

CHASSIS GROUND provides a terminal for connecting to the grounded amplifier chassis.

DANGER labeling in English and German warns of possible hazardous stored charges within the amplifier. Just below this labeling is a statement concerning an IEC approval restriction for this amplifier.

Interface Ports: To the left of the fuse bank are four control interface ports. Pin assignments for each port are listed in Appendix A. Three of the four ports, the external RF Monitor (RF MON), the Pulse Control Module (PCM), and the System Control Module (SCM), must be connected at all times for the MRI amplifier to function.

- **RF MON** is a safety interlock feature that connects to an external GE RF power monitor. Three pairs of lines are utilized for emergency shutdown of the amplifier of the RF monitoring device detects a problem. These lines are RFLCK–P and RFLCK–N, RFLCK*–P and RFLCK*–N, and HI VOLT REL (+ 12 VDC) and HI VOLT REL EN*. The remaining line pair (UNBW*P and UNBLK*–N) is used to echo the state of the PCM unblanking pins.

- **PCM** is dedicated entirely to a single pair of lines used to send the UNBLANK signal. UNBLANK enables the amplifier RF amplification stages. A BLANK logic signal (UNBW*–P greater than 1.5 volts with respect to UNBLK*–N) gates off the amplification.

- **SCM** allows the amplifier to be addressed by an external controlling computer. Operational commands are sent to the amplifier, and operational data may be read through this port. The SCM interface has been designed to comply with both of General Electric's BISYCL and BICYCLE links. Refer to Section 3.2.1 of Chapter 3 for information concerning SCM commands.

- **SERIAL PORT** allows for an alternate external computer interface. A separate set of commands is available for this interface. Refer to Section 3.2.2 of Chapter 3 for information concerning serial commands.

RF Connectors: The radio frequency (RF) input and output connectors are on the left side of the rear panel marked with the international "Attention" symbol (exclamation point within a triangle).

- **RF IN** is at the bottom right. This 50 ohm coaxial connector (BNC) is the only RF input port.

- **TEST RF OUT** at the bottom left is 50 ohm coaxial (BNC). When selected, this port provides a 100 milliwatt RF output intended for test purposes.

Section 1.3.1 Amplifier External Cabinet (Continued)

- **HEAD PORT** at the top left is type N–Female and outputs a 2.0 KW (maximum) amplified RF signal.
- **BODY PORT** at the top right is type HN–Female and outputs a 20.0 KW (maximum) amplified RF signal.

NOTE:

ALL coaxial lines should be 50 ohm characteristic impedance between amplifier and intended load.

The Erbtec logo and surrounding text located between the four coaxial connector pods contains Erbtec's address, the model number, the serial number, and the input power rating of the amplifier. All correspondence directed towards ERBTEC should go to this address. Include the model and serial number information as listed on the amplifier.

Section 1.3.2 Power–on/off Procedures

A summary of the entire power–up to power–down sequence of commands may be found in Table 1–1 in this Section. A description of this sequence follows. All commands are completely described in Chapter 3.

Power–On

The main breaker switch CB1 is located at the right side of the rear panel and is clearly marked ON/OFF (and 1/0). Turn main power ON to the amplifier by moving the switch to the ON position while viewing the front panel LED display (see Figure 1 –3).

Immediately after the switch is turned on, all LEDs on the front panel display briefly light. The amplifier then executes its power–on test. During this brief test, a "ker–chunk" sound is heard as the amplifier tests the tuning stepper motors. The internal power–on test is complete when all of the front panel LEDs turn off except for the OFF and BODY MODE LEDs (no fans are on). The amplifier remains in this state until instructed to proceed further. If the power–on test detects an irregularity, the test terminates with a lighted Fault LED and a Fault Code displayed. A complete listing of fault codes may be found in Chapter 4.

Standby

Following the main Power–on procedure, power–up proceeds with either a "power on" command or a "change mode" command followed by a "power on" command. The "power on" command may be issued through either the SCM interface or the serial port. This command will turn on the fans and initiate tube warm up. Warm up requires approximately six minutes to complete to allow tubes to reach a safe operating temperature. During warm up, the WAIT LED is it indicating the amplifier is inaccessible to further commands until this LED turns off.

Section 1.3.2 Power–on/off Procedures (Continued)

NOTE:

If a “power on” command is issued within fifteen seconds of the amplifier turning off from a warmed–up state, a much shorter wait time will occur (about 30 seconds).

WARNING:

High voltage comes up at the end of the wait period, and is on during both STANDBY and OPERATE modes.

Operate

The amplifier is ready to go into a full OPERATE mode when the WAIT LED turns off leaving only the green STANDBY LED and the BODY MODE or HEAD MODE LED lit. A “change mode” command may also be issued at this time. The amplifier is brought into a full operational (ready to amplify) state by issuing the “go to operate” command. The OPERATE LED will light when the amplifier is ready for unblanking conditions. Internal testing for irregularities is proceeding at all times, and shutdown automatically occurs if a problem is detected. Amplification of RF pulses requires a concurrent UNBLANK command from the PCM interface. See Table A–1 in Appendix A for PCM pin definitions and the Specifications in Section 1.2 of this Chapter for UNBLANK time requirements. During amplification of each RF pulse, the yellow UNBLANK LED is lit.

NOTE:

A “change mode” command is not accepted while the amplifier is in the OPERATE mode. If a change of mode is desired, the amplifier may be brought back into STANDBY by issuing a “return to ready” command; the LED display will change from OPERATE to STANDBY.

Power–Off

The amplifier may be placed into a power–off condition at any time by issuing a “power off” command. The yellow OFF LED is it as the amplifier power–down routine is activated. The entire shut–down routine requires a few seconds to complete, and the fans continue to turn during this time. The fans stop running when the power–down sequence is complete.

CAUTION:

All electrical power is removed from the amplifier ONLY by switching the main circuit breaker on the rear panel to the OFF marked position. ALWAYS unplug the main power cord before accessing the internal cabinet. Ground all parts and modules before touching. Wait several minutes before entering the internal cabinet if the amplifier has recently been in a power–on mode (including STANDBY).

Section 1.3.2 Power–on/off Procedures (Continued)

Table 1–1 Power–On/Off Cycle

PROCEDURE	SCM COMMAND (SERIAL COMMAND)	
Main Power–on	manually put main breaker switch CB1 to ON	
Select Mode (optional)	“change mode”	(“test” “head”, or “body”)
Standby	“power on”	(“o1”)
Select Mode (optional)	“change mode”	(“rest”, “head”, or “body”)
Operate	“goto operate”	(“o3”)
Standby (optional)	“return to ready”	(“o1)
Select Mode (optional)	“change mode”	(“test”, “head”, or “body ”)
Power–off	“power off”	(“o0”)
Main Power–off	manually put main breaker switch CB1 to OFF	

NOTE:
The leading character “o” in the serial commands is a lower–case letter o.

CHAPTER 2 THEORY OF OPERATION

Section 2.1 RF Signal Chain

The RF path through the amplifier may be broken down into essentially three subsections. In the first subsection, RF power of about a milliwatt (4 dBm +/–4 dB for max power out) or less enters the Solid State Amplifier where it is amplified to a level of 80 to 200 watts (49dBm to 53dBm) depending on the mode. In the second subsection, the RF signal enters the Vacuum Tube Amplifier Cavity (VTAC) where it is amplified by another 10 to 24 dB again depending upon the mode. In the final subsection, the RF signal passes through the RF Monitor module to detect forward and reflected power levels.

The three subsections are connected to one another through coaxial cables. The block diagram of Figure 1–1 illustrates the interconnection and basic functionality. The Solid State Amplifier is actually a single self–contained module (86–013–2500) as is the RF Monitor module (86–013–2800). The VTAC actually consists of several modules (86–013–2xx numbers and two tubes 176–100x), but the entire cavity can be viewed as a single subsection for descriptive purposes.

Each of these subsections is described individually in Sections 2.1.1 through 2.1.3.

Section 2.1.1 Solid State Amplifier

Overview

The Solid State Amplifier (SS amp) is a broad band linear amplifier capable of delivering up to approximately 400 watts maximum peak power (with a duty cycle of a few percent). In the MRI amplifier, the SS amp is utilized to deliver a nominal 80 watts BODY mode or 160 watts HEAD mode to the VTAC at a center frequency of 63.86 Mhz. All RF inputs and outputs are 50 ohm characteristic impedance.

The SS amp essentially functions as a quality preamp for the high power RF tubes in the VTAC. The linearity, bandwidth, and noise performance of the SS amp must meet or exceed overall amplifier performance goals in order to meet linearity, bandwidth. and noise specifications.

A simplified functional block diagram of the Solid State Amplifier depicting all primary functions is shown in Figure 2–1. The SS amp schematics (number 86–013–2510) are located in Chapter 5 of the *Service Manual*.

Section 2.1.1 Solid State Amplifier (Continued)

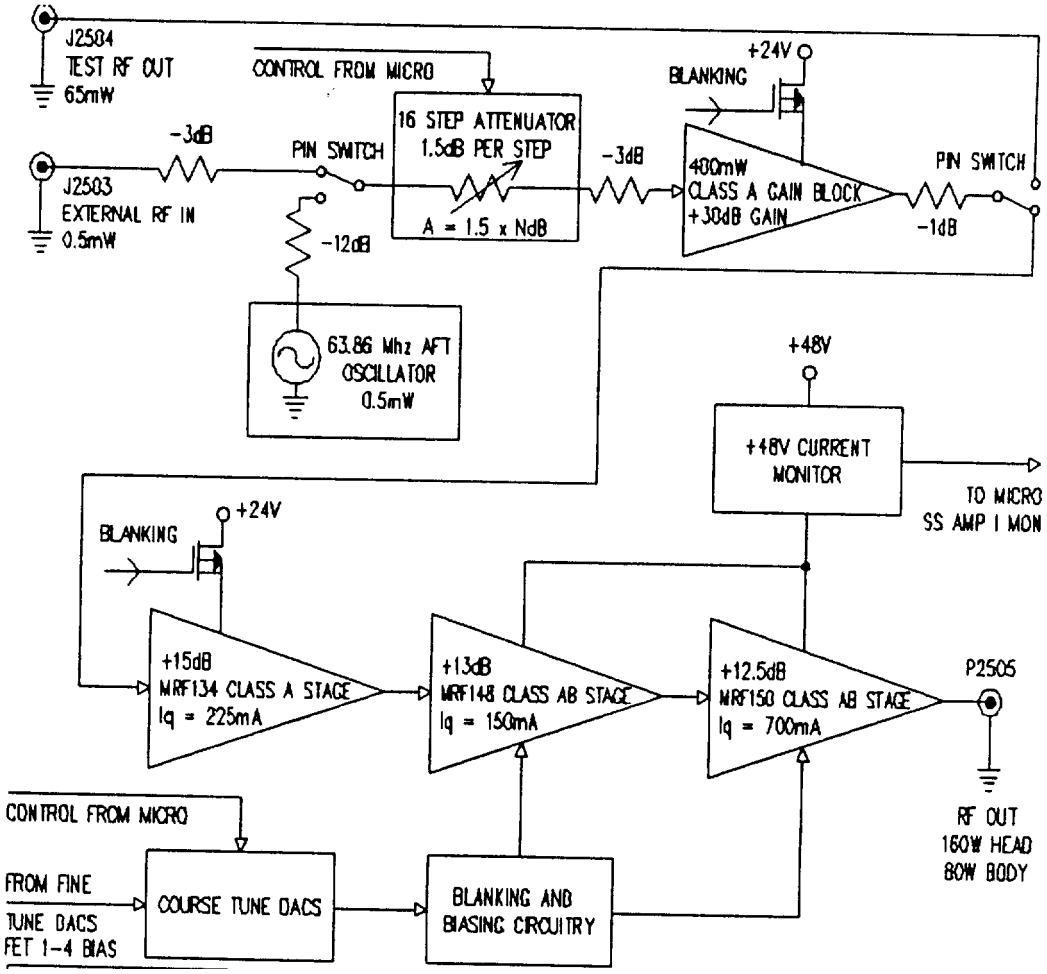

Figure 2–1 Solid State Amplifier Functional Block Diagram

RF Input Path

Pulsed RF enters the amplifier through 50 ohm BNC connector J2503 RF IN (see schematics). Typical maximum output power occurs for an input power level of about 0.4 milliwatts (–4dBm +/–4dB). Immediately after entering the SS amp, the RF signal encounters a pi–resistance network (R101. R102, and R103) which provides 3 dB of attenuation and improves the 50 ohm input impedance match. The signal then proceeds to a PIN diode switch (EXTRF) which routes the signal either to ground (through 50 ohm resistor R97) or on to the step attenuator. The ground path is enabled if the on–board oscillator has been digitally selected for automatic fine tuning (AFT) purposes. Normally, the signal proceeds to the step attenuator circuit.

Section 2.1.1 Solid State Amplifier (Continued)

Step Attenuator

An on–board attenuator with a range of 0 to 22.5 dB in 1.5 dB steps is incorporated to account for production gain variations in boards and to control power levels to the tube cavity for the different modes of operation.

The attenuation is accomplished with four 50 ohm pi–resistor networks attenuating 1.5, 3, 6, and 12 dB respectively. This combination allows for attenuation selection in 1.5 dB increments from 0 to 22.5 dB by using sequential combinations of the four cells. individual cells are selected or bypassed digitally using the signals A0, A1, A2, and A3, which control PIN diode switches. These digital signals are the last four bits of the “solid state serial latch” (see microprocessor theory and diagnostics).

Typically, there is 7.5 dB of attenuation selected (the 1.5 and 6 dB cells on) for HEAD mode allowing about 150 to 200 watts full power into the VTAC. Another 3 dB (10.5 dB total) is added for the BODY mode allowing about 75 to 100 watts full power into the tube cavity Production SS amp boards do not vary by more than +/– 1.5 dB in overall gain.

30 dB Gain Block

Following the step attenuator, the RF signal (labeled TRW IN on the schematic) passes through another 3 dB attenuator (R113, R114, and R115), an IC gain block (A1), and the final 50 ohm attenuator (R117. R118, and R119) which attenuates by 1 dB to provide output impedance matching for the gain block. The IC gain block is a wideband, low noise, linear hybrid class A amplifier with gain very near 30dB at 64 MHz.

For an input power level of –4 dBm, the values discussed thus far yield a nominal power level of about +11.5 dBm for the HEAD mode at the output of the 1 dB attenuator (R119) neglecting any insertion losses (3dB less for BODY mode).

TEST Mode

The RF signal then proceeds to the last of the digitally controlled PIN diode switches (EXTOUT). This either switches the RF signal on to the FET stages for normal amplification or to the J2504 TEST RF OUT connector.

In the TEST mode, the attenuator cells are all switched on (bypassed). This results in a full power of about 18 dBm (+/– 1 dB) on the connector (for input of 4 dBm). In a lossless system, about 19 dBm would be expected; this indicates that about 1 dB of insertion loss exists in the RF path discussed so far.

Section 2.1.1 Solid State Amplifier (Continued)

Class A FET Stage

if either the BODY or HEAD modes are chosen, the RF signal proceeds to a class A amplifier consisting of two MRFl34 field effect transistors (FETs) (O23 and Q24). Just prior to the gates of these FETs, the signal is split into two equal signals 180 degrees out of phase by transmission line transformer T1. Thus half of the available power appears at each gate of the MRF134's. In practice the two gate (or drain) signals may vary by a few percent (on all FETs).

The MRF134 provides about 16 dB of gain for the power supply voltage and frequency used in this application. The power output from the class A stage is recombined in phase through transformers T2 and T4 which also perform impedance transformation along with T3 and T5. A 50 ohm impedance point exists midway between the T2/T4 and T3/T5 transformer pairs.

Theoretically, a HEAD mode power level of 11.5 dBm (RF signal at R119) minus 1 dB insertion losses minus 3 dB for power split across the two MRF134s plus 16 dB gain of MRF134 plus 3 dB recombination gain of two MRFl34 outputs yields 26.5 dBm (about 450 milliwatts) at the input of the MRFl48 gain stage.

MRF 148 Class AB Stage

Transmission line transformer T5 splits the class A stage power output across two MRF148s (O25 and O26) and also transforms the impedance level to about 12.5 ohms. The MRF148 FETs are biased in a class AB mode (emphasis on B) and operated in a push–pull manner through transformer T6.

The MRF148s have a gain on the order of 16 dB. Therefore, a power level of 26.5 dBm (after class A stage) minus 3 dB for power split across MRF148s plus 16 dB gain of MRF148 equals 39.5 dBm (8.9 watts) should ideally exist at the input of the MRF150 gain stage. There is not a 3 dB recombination gain after the MRF148s since the FETs are push–pull. A 50 ohm impedance point exists between T6 and the T7/T19 pair.

Class AB MRF 150 Stage

The transformer pairs T7/T9 and T8/T10 perform a 16:1 impedance transformation down to about 3.125 ohms to closely match the input impedance of the two MRF150 FETs (O27 and O28). These FETs are also biased in a class AB mode and operated push–pull through transformer T11. Transformers T12 and T13 step up the impedance to 50 ohms at the output connector P2505.

The MRF150s have a power gain on the order of 17 dB yielding a HEAD mode theoretical output power of 39.5 dBm (output of MRF148 stage) minus 3 dB power split across the MRF150s plus 17 dB gain of MRF150 equals 53.5 dBm (about 220 watts). In practice, the HEAD mode power out is typically observed to be between 51 and 53 dBm for a 4 dBm input (3dB less for BODY mode).

Section 2.1.1 Solid State Amplifier (Continued)

FET Biasing

Erbtec has developed a proprietary method of biasing amplifier elements (transistors and tubes) called “Dynamic Bias and Refresh”. This biasing technique is utilized in the two class AB FET stages and partially in the VTAC (dynamic bias only). Section 2.2, *MicroProcessor Controller* also contains a discussion of the technique.

The class A MRF134 stage is manually biased to 225 milliamps by factory–set potentiometers. Since the bias of this stage is manually set and fixed, the small drift in bias currents due to temperature, aging, and component variation common to most amplifiers will occur. However, this drift should not significantly affect the performance of parameters such as linearity and bandwidth due to the class A bias.

The MRF148 and MRF150 stages are class AB (with emphasis on the B). Bias currents of 150 milliamps and 700 milliamps for the MRF148s and MRF150s respectively provide the best operating points. It is highly desirable to keep the operating point constant for these stages. Therefore, the SS amp invokes a digitally controlled biasing network to set and “refresh” the bias. The microprocessor continuously monitors the FET DC drain currents, and makes fine adjustments on the gate voltages to keep the operating points at their optimum.

FET gate bias voltage is controlled with two microprocessor–adjustable voltages. These voltages are called the coarse and fine adjust. The fine adjust voltage consists of signals labeled FET1 BIAS – FET4 BIAS and is used to very finely adjust the gain of the LF356 opamps (U1–U4) by floating the “ground” reference of the opamp’s resistor feedback loop at the 1.82 kiloohm resistors (R12, R2, R7, and R17). The voltage across these resistors is varied from 0 to 0.4 volts by the application of 0–20 volts at the FET14 BIAS lines via Processor Board DACs.

These 0–20 volt Processor Board DAC voltages also serve as on/off switch references for UNBLANK and BLANK through LM338 comparators (U5A–D). The voltage level at the positive terminal of the comparators can range from 0 to 4 volts. An UNBLANK logic signal (RF GATE on the SS amp schematics) drives the minus pin of the comparators (FET ENABLE) low (around 0.6 volts). A comparator + terminal voltage greater than FET ENABLE causes the comparator output to go open–collector (high impedance). Conversely, a logic BLANK signal places the FET ENABLE line at about 4.5 volts, and the comparator outputs go to a logic low state (saturated transistor).

The positive inputs of the LF358 opamps are tied to both the comparator outputs and the outputs of a 5 volt, 6 bit DAC (U6) which serves as the coarse adjust voltage. When the comparators are logic low (BLANK), the coarse DAC voltage is virtually grounded out. When the comparators are logic high, the LF358 opamps provide a finely adjustable +2 voltage gain for the coarse adjust voltage. Therefore, a high–resolution variable FET gate voltage of 0 to 10 volts is applied and controlled by the microprocessor.

Section 2.1.1 Solid State Amplifier (Continued)

NOTE:

FET gate voltage equals 2 x (coarse DAC volts) – (fine DAC volts) or (0.159 x #coarse bits) – (0.0014 x #fine bits) where #coarse bits is 0–63 and #fine bits is 0–255.

The initial biasing of the MRF148 and MRF150 FETs begins just as the amplifier is going into STANDBY. The fine bias voltage is set to the low end of its range, but sufficiently high to force the comparators to go open–collector when UNBLANK occurs. The microprocessor then issues an UNBLANK, and adjusts the course DAC to the first bit that produces a DC bias current above the target value. The fine adjust voltage is then increased to lower the LF356 opamp gain until the bias current is lowered to precisely the target value.

Refresh biasing occurs continuously while in both STANDBY and OPERATE (between UNBLANK pulses). The microprocessor checks the bias current of each FET and adjusts the fine voltage DAC as necessary to maintain the optimum operating point.

Bias Current Transducer

To dynamically set and refresh the FET bias currents, the microprocessor must be able to accurately monitor their DC bias currents. This function is performed with a current to voltage transducer consisting of D1, R33, R31, U7, Q1, and R29. The transducer uses opamp U7 to actively sense the FET current (divided by 100) drawn from the 48 volt rail. Q1 is used as a voltage controlled current source and passes on the scaled FET current, but limits the amount of current passed when it gets too high.

Q1 has a specified gate threshold voltage in the range of –2 to 4.5 (Vgs). Therefore, the opamp output must remain at least 4.5 volts (worst case) below the source voltage for Q1 to remain on. The opamp is operated 15 volts differentially across the 48 volt supply with 15 volt zener diode D1. Therefore, the low voltage swing of the opamp is near 33 volts, and the source of Q1 must be at least 37.5 volts to ensure Q1 is fully on. This implies that a maximum current of approximately 10.5 milliamps can pass through R30, R31 and Q1, or the transducer has a maximum accurately measured FET current of 1.05 amps. The current passed through Q1 is converted to a voltage by R29 for A/D sampling by the microprocessor.

Since the maximum FET target bias current is 0.7 amps, the current transducer must sample each FET individually to prevent saturation of the current transducer (keep Q1on). This is accomplished by issuing an RF GATE signal (UNBLANK) and putting all FETBIAS lines to zero except for a single FET. Since FET ENABLE is about 0.6 volts, an FETBIAS of 0 volts keeps the LM339 comparator outputs low. Under normal operation when UNBLANK occurs and RF is present, the total 48 volt supply current can be as high as15 amps peak, and the transducer is saturated. Therefore, refresh is only done while no RF is present.

The resolution of the current transducer is limited by the microprocessor A/D sampling at R29. This resolution is about 0.02 volts per bit (5 volt, 256 bit) which corresponds to about 5 milliamps per bit through R29.

Section 2.1.1 Solid State Amplifier (Continued)

Digital Control

The microprocessor communicates to the SS amp and LED display boards through the "serial peripheral interface." The details of timing and data transfer are covered in Section 2.2, *Microprocessor Controller*. The majority of the digital control on the SS amp is performed by chip U9, an 8 bit shift register with a gated output latch. Data is shifted through this device and on to the coarse adjust DAC (signal labeled DATA) with the last 8 bits of data held in the gated output latch. These last 8 bits control the attenuators (least significant 4 bits labeled A0–A3), the internal/external RF path selection (INTRF, EXTRF, the TEST mode output (EXTOUT), and the oscillator on/off switch (OSC).

Oscillator

The NMR amplifier uses a 63.86 MHz oscillator on–board the SS amp to perform AFT each time the amplifier goes into OPERATE. The oscillator circuit consists of Q2, L1, C38, C39, R49, and crystal X1. The configuration is common–base with a third overtone series resonant crystal (X1) feeding the emitter of Q2. Fine frequency and amplitude tuning is accomplished with variable inductor L1 which is adjusted at the factory for optimum oscillator output at 63.860 MHz. Components C49, C50, L2, and C63 form a band–pass filter to reduce harmonic output, and the pi–resistor network R93, R94, and R95 provides a 50 ohm 12 dB attenuator.

The oscillator is digitally gated on when the OSC signal goes high (+5 volts). Resistors R48 and R50 provide the DC bias voltage at the base of Q2. Capacitor C37 is an RF bypass capacitor which causes the base of Q2 to appear at essentially RF ground.

The output power of the oscillator is roughly equivalent to applying an RF input signal of –8 dBm at the J2503 RF IN connector.

Temperature Monitor

The temperature of the SS amp is monitored via a resistance divider using thermistor RT1 and resistor R123 on the Processor Board. At 25 degrees Celsius (77 Fahrenheit), the resistance of the thermistor is specified at 10 kohms. This puts a nominal voltage of 2.5 volts at the HS MON pin of P2501 for the microprocessor to monitor. The microprocessor will issue a temperature fault at 4 volts and 1 volt which roughly corresponds to –4 and 60 degrees Celsius (25 and 140 degrees Fahrenheit) respectively. The voltage versus temperature characteristics of the thermistor are very nonlinear. This makes it difficult to use the thermistor as a temperature indicator, so it is used only for indication of temperature extremes.

Section 2.1.2 Vacuum Tube Amplifier Cavity

Overview

The vacuum tube amplifier stages are grounded grid and tuned (resonant) class AB2. In the HEAD mode only the Intermediate Power Amplifier (IPA) tube, EIMAC ceramic triode type 3CPX800A7, is used. In the BODY mode the IPA stage is operated at 3dB less power by increasing the Solid State Amplifier attenuator and drives the cathode of the Power Amplifier (PA) tube, EIMAC ceramic triode type YC156. The 3CPX800A7 tube is a high voltage version of the more familiar 3CX800A7. However, the YC156 tube should not be confused with other tubes of similar physical size. The anode is similar to other 5 KW dissipation external anode tubes, but the cathode is derived from the much larger 3CX15000B7 tube to maintain large cathode emission reserves for long MRI pulses.

NOTE:

In this Section the engineering term “resistive” corresponds to the mathematical term “real”; similarly, the term “reactive” corresponds to “imaginary”. Unless otherwise specified, all references to the terms resistive and reactive are with respect to the conventional series equivalent impedance format.

The amplifier is tuned at the factory to provide full rated power under the worst–case 10% low line voltage. The criteria used for tune–up is 0.6dB/dB compression when incrementing 1dB from 2 KW (HEAD mode) or 20 KW (BODY mode). Significantly more power is available if overdriven at 10% high line voltage. However, a forward power limit is imposed by the RF Monitor module and causes the amplifier to return to STANDBY should the forward power limit be exceeded (BODY limit is 27 kilowatts; HEAD limit is 3 kilowatts).

A functional block diagram of the VTAC and RF Monitor is shown in Figure 2–2.

IPA Stage

RF power from the Solid State Amplifier enters the Vacuum Tube Amplifier Cavity (VTAC) at BNC connector J2601 connected to the IPA Input Board (schematic 86–013–2611). The 50 ohm system impedance is transformed up in the ratio of 1:4 by broadband transformer T5 on the IPA Input Board. The Solid State Amplifier is terminated in its design center load impedance of 50 ohms resistive when a 200 ohm resistive load is presented to the secondary of T5.

Inductor L5, capacitors C24, C20 and C23, and 50 ohm transmission line W1 form a resonant PI tank circuit. The tank circuit transforms the 33 ohm (approximate) resistive input impedance of the IPA tube to present a 200 ohm resistive load to T5. The shunt input capacitance of the IPA tube is in parallel with W1, C20 and C23, so capacitive variations from tube to tube are minimized. The technique of transforming up to a higher impedance value and then down to a lower value of system impedance is invoked to utilize practical values of components and suitable circuit Q’s for energy storage during the non conducting portion of the tube RF input cycle.

Section 2.1.2 Vacuum Tube Amplifier Cavity (Continued)

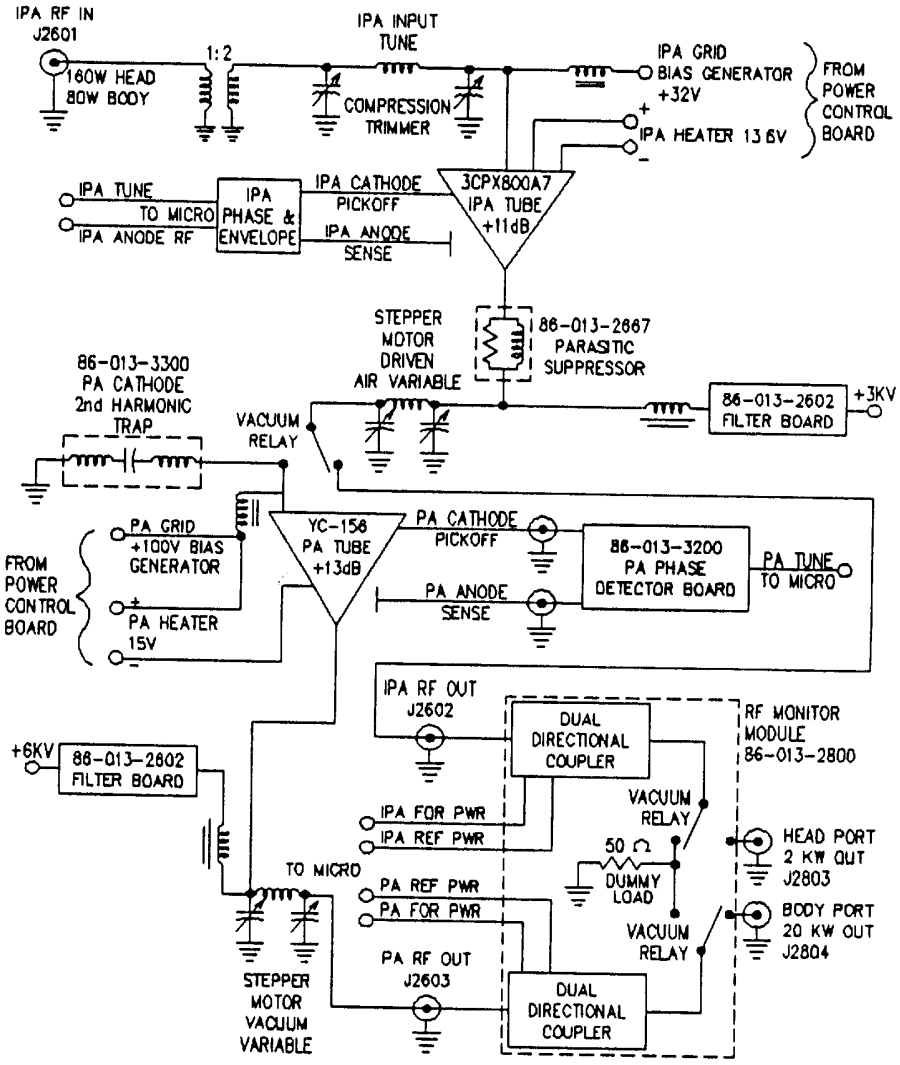

Figure 2–2 VTAC and RF Monitor Functional Block Diagram

During factory tune up, variable compression trimmer capacitors C24 and C23 are set to provide minimum reflected power (typically –30 dBc or better) to the Solid State Amplifier. These capacitors should not be disturbed in the field without full reflected power and bandwidth measuring capability.

IPA tube cathode DC bias enters the VTAC via in–line bypass capacitor C3 and ferrite RF chokes L1 and L3. Capacitor C18 is used to isolate DC signals between the Solid State Amplifier and the IPA stage. C7 is a bypass capacitor, and D1 is a high current diode used to protect the bias circuitry should an internal arc occur within the IPA tube.

Section 2.1.2 Vacuum Tube Amplifier Cavity (Continued)

NOTE:

An occasional tube arc (between anode and grid) can occur, particularly when a tube is brand new. The phenomenon is normally self healing when suitable energy limiting circuits are employed.

The heater voltage (13.6 VDC) for the IPA tube enters the VTAC via in–line bypass capacitors C1 and C2 and connects to the IPA Tube Socket assembly through biflar wound ferrite chokes T1 and T2 and the twisted wire pair (red/black) W3A and W3B. Capacitors C5 and C6 are RF bypass capacitors.

The DC IPA tube anode supply (+3 KVDC nominal) enters the VTAC (see overall VTAC schematic 86–013–2610) via its own cable and is applied to the IPA tube anode through the VTAC Filter Board (86–013–2602) and RF choke L9 (86–013–2635). Capacitors C6 and C7 provide high voltage DC blocking and RF bypass.

RF power from the IPA tube anode is coupled to the anode tank circuit via a parasitic suppressor (86–013–2667) consisting of a metal strap inductor shunted by four carbon composition resistors. Motor driven air variable capacitors C1 and C2 and sheet metal inductors L3 and L4 form the tank circuit. The tank transforms the approximate 17 ohms resistive input of the PA tube in BODY mode or the 50 ohm load impedance in HEAD mode to the design–center IPA anode load line of 850 ohms resistive.

IPA stage output power is routed out when operating in the HEAD mode or on to the PA stage when in BODY mode via vacuum relay K1 (on the PA Input Board). The HEAD mode output passes through sheet metal inductors L5 and L6 (overall cavity schematic) and on to the type N connector J2602 mounted on the VTAC endplate.

PA Stage

In both HEAD and BODY modes, series–connected ferrite chokes L1, L2 and L3 on the PA Input Board (schematic 86–013–2613) are present to provide a direct high current path to ground in the event of a short circuit failure of the IPA anode DC blocking capacitor. Diode D1 is a tube arc protection diode. Other components on the PA Input Board also perform very similar functions as on the IPA Input Board. Capacitor C9 is a DC block; L4, L5, C1 and C6 decouple the RF from the PA tube cathode DC bias. Bifilar wound chokes T1 and T2, together with capacitors C2, C3, C4, C5, C7 and C8, decouple the PA tube cathode RF from the PA heater supply.

PA input shunt capacitance variations are absorbed in a similar manner as for the IPA input stage (swamped by input tank). Note that the cathode of the PA tube is connected internally within the tube to one end of the heater winding. The heater supply is designed to float, with respect to ground, and its potential tracks the pulsed (BLANKED/UNBLANKED) DC cathode bias voltage.
The YC–156 PA tube has no specific mounting socket with pins (see overall VTAC schematic 86–013–2610). Instead, the silver–plated copper mounting flange provides the grid connection directly to ground, and the cathode and heater connections to the tube are made with machine screws that pass through matching holes in the cathode strap and heater wires respectively.

Section 2.1.1 Vacuum Tube Amplifier Cavity (Continued)

A series–resonant second harmonic trap (86–013– 3300) is also attached between one of the four cathode terminals and chassis ground. Capacitor C11 connected across the heater wires at the tube and capacitors C11 and C12 (on the PA Input Board) are used to couple the RF potential at the cathode to the PA CATHODE PICKOFF for phase detection.

PA tube anode supply voltage (+6 KVDC nominal) enters the VTAC via its own cable and is connected to the PA tube anode through a VTAC Filter Board and high voltage RF choke L9. Capacitor C5 is a high voltage RF bypass capacitor.

RF output from the PA anode passes first through inductor L8 and DC blocking capacitors C8, C9 and C10 connected in parallel to handle the high circulating RF currents present. RF choke L12 provides a low resistance DC path to ground in the event of short circuit failure of any of the DC blocking capacitors. As for the IPA stage, a tank circuit transforms the 50 ohm BODY load impedances to the PA tube resistive load line design–center of 394 ohms. The tank circuit consists of sheet metal inductors L10, L11 and L13, and motor–driven vacuum variable capacitors C3 and C4.

The shunt output capacitive reactance of the PA tube is significant at the operating frequency. Therefore, this tank circuit should be considered to be a PI–PI–L configuration. The BODY output appears at the type HN connector J2603 mounted on the VTAC endplate.

Automatic Fine Tune (AFT)

Replacement of vacuum tubes in the field ordinarily results in slight mistuning due to tube variations. The amplifier uses phase detectors to automatically correct the tuning every time the amplifier is commanded from STANDBY to OPERATE.

The definition of correct tune, as used herein, includes centering the passband around 63.86 MHz. Conventional fine tuning done by searching for amplitude peaks is both insensitive and inaccurate since peak output power at the center frequency is not necessarily co–incident with bandwidth centering. In addition, amplitude linearity can be degraded when a resonant amplifier is tuned solely to meet a maximum power output criterion. Instead, a phase detector placed between cathode and anode is used.

The phase detection circuitry used in this amplifier exhibits a well defined polarity reversal (DC signal goes from one side of “zero–phase” reference to other side; zero–phase reference level is 2.5 volts DC) when the load is tuned through the desired purely resistive condition.

Both the IPA and PA stages use similar phase detector circuits. The main difference between the two is the incorporation of the IPA phase detection circuit into the IPA Input Board, whereas the PA Phase Detector is a stand alone unit mounted outside of the VTAC in the Processor Cavity. Both phase detectors are fed by a coaxial cable from an anode pick–off board near each tube in the VTAC. Only voltage sensing is used since current sensing is inaccurate due to the circulating currents caused by tube capacitances (particularly in the case of the PA stage).

Section 2.1.2 Vacuum Tube Amplifier Cavity (Continued)

The cathode RF potential is sampled by a capacitive voltage divider in which the ground referenced capacitor has a small reactance (one fourth or less) compared to the designed circuit impedance of 50 ohms. The anode RF potential is sampled by the anode sensing (pick–off board. This device is really a small high voltage capacitor consisting of one layer of foil on a PC board making up one plate of the capacitor, an air gap between the board and the tube, and the anode structure of the tube acting as the other capacitor “plate.” The same PC board is used for both IPA and PA stages, but the air gaps are different to accommodate the different RF potentials and tube structures.

The foil on the PC board is connected via a 50 ohm coaxial cable through a balun transformer to a 50 ohm center tapped load in the phase detector (R6 and R7 for the IPA, R2 and R4 for the PA). Because the reactance of the small anode coupling capacitor is very large compared to the load resistor, the phase of the voltage across the center tapped load is rotated by nearly 90 degrees from the anode RF potential. The coaxial cables that connect the cathode and anode sensors to the phase detectors are cut to lengths such that their respective phase shifts cancel. Production tolerances are accommodated by trimmer capacitor C28 on the IPA input board and by firmware for the PA stage.

The cathode RF sample which appears across resistor R5 on the IPA Input Board and resistor R3 on the PA Phase Detector Board is not substantially rotated in phase. The cathode sample is applied to the center tap of the anode sample load resistors (24.9 ohm, 1% for both circuits). The vector sums of the RF samples are detected (rectified) by Schottky diodes D1 and D2 for the PA and D8 and D9 for the IPA, and the algebraic sum appears across series connected DC load resistors R1 and R5 for the PA and R2 and R3 for the IPA.

DC potential across the phase detector load resistors can vary between positive and negative values; therefore, the reference end of the load is raised to a nominal 2.5 volts by resistor dividers. Resistors R6 on the PA, R4 on the IPA, and similar resistors on the Processor Board connected to +5VDC form the dividers. The remaining capacitors and inductors provide RF bypassing and ripple filtering. In the PA Phase Detector, diodes D3 through D7 in conjunction with R7 limit the peak swing of the phase detector output to safe input levels for the microprocessor A/D. The IPA phase detector functions identically.

When the amplifier is correctly tuned, the phase detector output signal is at zero volts with respect to the nominal 2.5 volt “zero” reference level. AFT is automatically performed during each STANDBY to OPERATE transition. RF input from the 63.86 MHz oscillator located on the Solid State Amplifier Board is applied to the VTAC stages. The microprocessor reads the phase detector output voltage and steps the appropriate “tune” motor (Motor 1 for IPA or Motor 3 for PA) with attached variable capacitors until a zero signal condition is achieved.

During the AFT process the output power for the mode selected is diverted to a 50 ohm load within the RF Monitor Assembly. This ensures a resistive load to the amplifier stages and keeps the AFT signal from the external MRI system. AFT uses a power level about 9 dB below maximum rated peak output power for BODY mode and about 6 dB down for HEAD mode.

Section 2.1.3 RF Monitor

Overview

VTAC RF output power from type N connector J2602 (HEAD mode) and type HN connector J2603 (BODY mode) on the VTAC endplate is routed into the RF Monitor (schematic 86–013–2812) via RG393 coaxial cables. This module monitors forward and reflected power for each mode and also provides the 50 ohm load for AFT. Figure 2–2 in Section 2. 1.2 shows a functional block diagram of the module.

Also mounted on the chassis is one of the two safety–interlock cover switches (SW1) used for safety protection when the amplifier's side covers are removed. The other switch is located in the AC switching Module.

Power Monitoring

The RF Monitor module contains two dual directional couplers, one for HEAD and one for BODY. Detector circuits produce DC voltage analogues of the forward and reflected power. The directional couplers and detector circuits are identical for both HEAD and BODY modes, with the exception of scaling resistors R6 and R7 (HEAD) and R14 and R13 (BODY). RF paths through the RF Monitor are selected by relays K1 and K2.

The dual directional couplers are of an Erbtec proprietary design that uses a 65 ohm printed microstrip transmission line (on the back side of the PC board) in shunt with a 220 ohm air spaced transmission line on the top side of the board. The 220 ohm branch line acts as a –12 dB coupler and also carries a toroidal current transformer that acts as a –26 dB transmission line (backwards) coupler. The sum of the two transmission lines is 50 ohms, and does not perturb the main system impedance. In this manner, a matched –38 dB broadband directional coupler is achieved.

The 220 ohm branch line is formed from a short length of RG393 coaxial cable with both ends of the outer braid removed. The remaining braid (about 1 1/2 inches) forms a small high voltage capacitor with the center conductor. Because it is almost at ground potential due to C4, C10 and R2 (HEAD mode), it acts both as a Faraday shield and the upper leg of a voltage divider. The junction of these points is connected to the center tap of two 24.9 ohm resistors (R1 and R3) placed across the toroidal current transformer.

The vector sum of the voltages appearing across R1 and R2 resulting from the forward power entering the HEAD mode via cable W2 is rectified by diode D1 and filtered to produce a DC analogue signal. The DC signal is passed to the microprocessor via P2802 and P2801. In a similar fashion, reflected power is detected by D2 and associated circuitry. Trimmer capacitor C4 is adjusted during factory calibration for maximum directivity of the forward power measurement (typically 30 dB or better) and potentiometers R4 and R5 are set to provide 4.00 VDC at 2 KW (HEAD mode) for both forward and reflected power sampling by the microprocessor A/D.

Section 2.1.3 RF Monitor (Continued)

The factory BODY mode adjustments are identical except that the power level corresponding to 4.00 VDC is 20 KW. Diodes D3 through D6 together with zener diode D5 clamp the voltages to a safe level for the microprocessor A/D.

The forward over–power fault trip point is set by firmware to be midway between the voltages that correspond to the rated power output and the maximum allowable power output. The reflected power trip point is set by firmware at the voltage corresponding to a 9:1 VSWR. See Section 2.2, MicroProcessor Controller for a table of fault limits.

During OPERATE, the RF Monitor mode not in use is terminated into the 50 ohm, 90 W, AFT resistor (R20). This feature allows for a port to port isolation of about 60 dB. RF power to the external MRI system is delivered to type HN connector for BODY mode and type N connector J2803 in HEAD mode on the amplifier rear panel.

Section 2.2 Microprocessor Controller

Overview

The amplifier controller is physically located behind the AC Switching Module on the Processor Board (86–013–2200). This board is responsible for maintaining the characterization data such as serial numbers, gain corrections, and tuning parameters that customize the amplifier.

The microprocessor acts as the center of amplifier internal and external communications including interpretation and response to both SCM and RS–232 commands. The microprocessor also monitors and controls the overall performance of the entire amplifier. Control includes start–up of power supplies, tube and transistor bias, and fault detection.

A simplified function block diagram of the Processor Board is provided in Figure 2–3. Consult schematic set 86–013–2210 for the location and configuration of components mentioned in this discussion.

Central Processing Unit

The amplifier uses an MC68HC11 as the central intelligence device. This chip is an 8–bit microcontroller with on board ROM, RAM, and EEPROM. The controller also addresses (In a 16–bit bus address mode) 16k of external EPROM containing the configuration data, coded routines, etc., as well as a 255 byte dual port RAM. Other useful features of this microcontroller include an enhanced 16–bit timer system, an 8–bit pulse accumulator, an asynchronous serial communications Interface (SCI), a synchronous serial peripheral interface (SPI), eight on– board 8–bit A/D converters, Computer Operating Properly (COP) watchdog system, and several options of interrupt configuration.

Section 2.2 Microprocessor Controller (Continued)

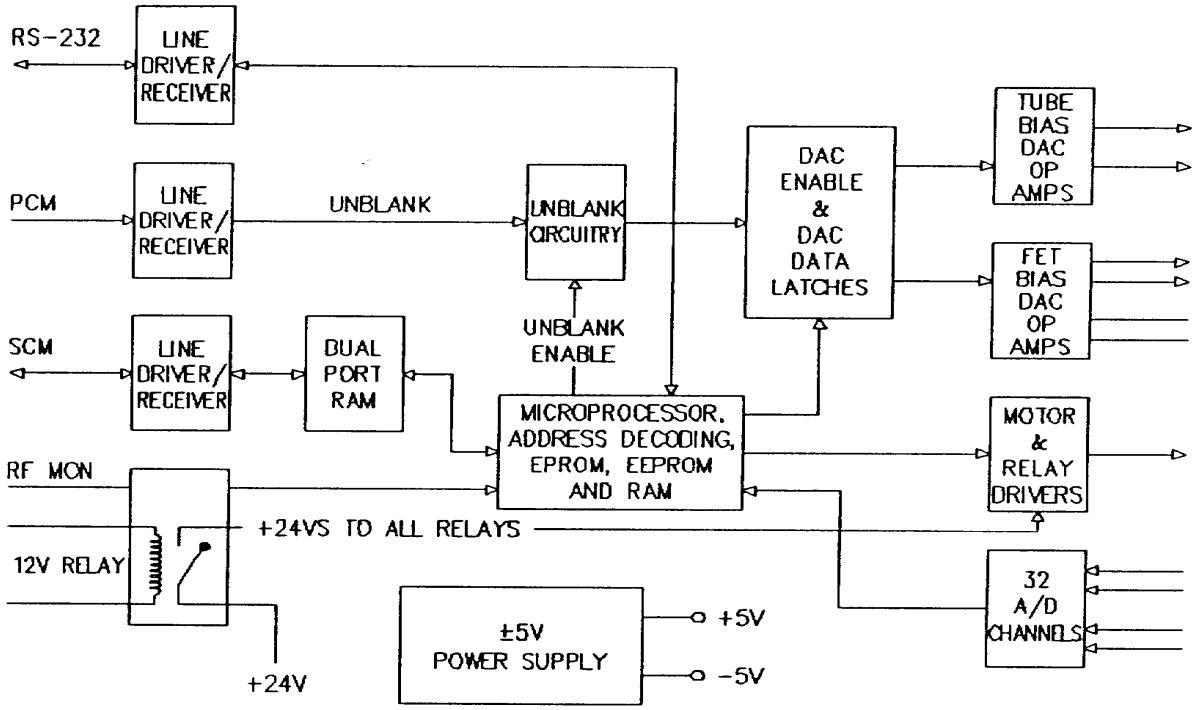

Figure 2–3 Processor Board Functional Block Diagram

The microcontroller can be configured to operate in one of four modes depending upon the state of MODA (pin 24) and MODB (pin 25) at power on. In the amplifier these two pins are set high (at power on) resulting in the “external address” mode. The controller system E–clock is configured to operate at 2 MHz.

NOTE:

The Motorola technical data manuals should be consulted for more detailed information on the specifics of operation and labeling used in this Chapter, Chapter 3, and Chapter 4.

Section 2.2 Microprocessor Controller (Continued)

Several significant configuration registers on–board the microprocessor (starting at address 1039h) serve to completely describe the configuration of the microprocessor for this amplifier. The OPTION register is loaded with 92h, which enables usage of the eight on board A/D converters, the A/D to be driven by the E clock, IRQ to be level sensitive, a 4064 E–clock delay mode, disables clock monitor, and sets CCP time–out period to E clock divided by 16. The HPRIO register is loaded with 2Dh, which affirms the MODA/MODB configuration, and sets a “timer output compare 3” mode for priority of the I input interrupt. The INIT register is loaded with 1 h, which sets the default starting address of RAM to 0000h and starting address of the 64 control registers to 1000h. The CONFIG register is loaded with 09h, which disables the security mode, enables the COP watchdog, disables the on board RDM, and enables the on board EEPROM.

A complete description of firmware and addressing is found in Chapter 3. Consult that Chapter for details about addressing and allocation.

The Processor Board communicates with the Solid State Amplifier (86–013–2500) and the Front Panel Display Board (86–013–2300) through the synchronous serial peripheral interface (SPI) bus. In this amplifier the SPI is configured as the Master and utilizes the MOSI mode to transmit data on this bus from the Processor Board to the target board. The bus consists of the two signals “data out” (valid on falling edge of clk) and “clk out” at 500 KHz. The data may be divided into three signals for characterization, SS latch, Segment latch, and Status latch. The SS latch is gated by a logic high on the ATTN line on the Solid State Amplifier Board; this latches the data transmitted over the SPI (MOSI line) into the Soiid State Amp. Similarly, the Segment latch and Status latch correspond to the logic lines CODE and STAT respectively on the Front Panel Display Board. These function in precisely the same way to latch data (MOSI1 line) to the seven–segment display and the status LEDs.

Figure 2–4 illustrates the timing diagram for a single byte data transfer. Figure 2–5 illustrates the more complicated byte structure required to set the course DACs for the FET biasing (see the Solid State Amplifier theory of operation in Section 2.1.1) and the PIN diode switch control byte.

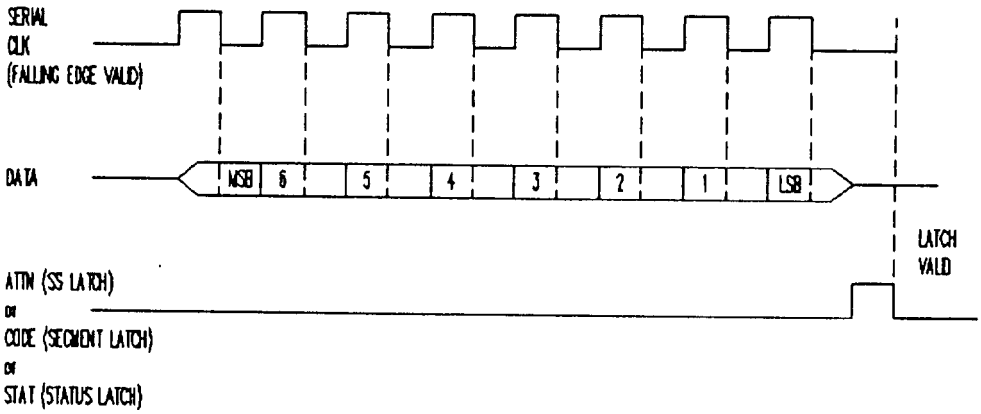

Figure 2–4 SPI Latch Timing Diagram

Section 2.2 Microprocessor Controller (Continued)

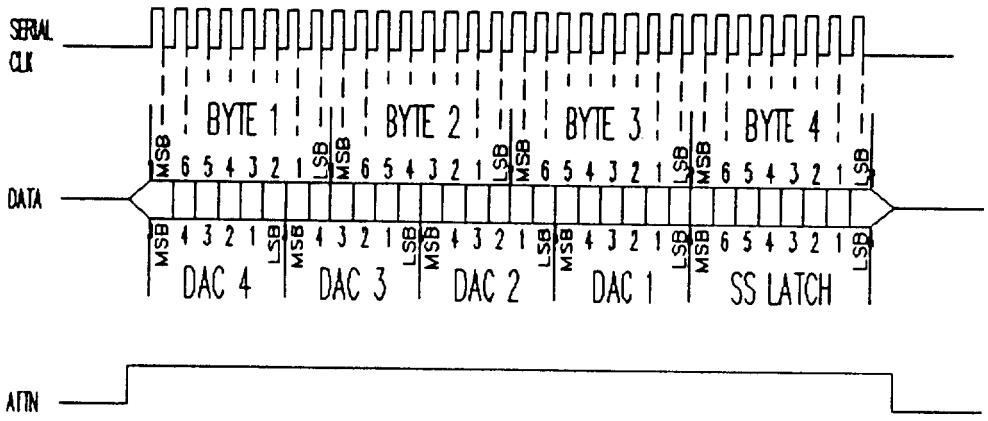

Figure 2–5 SPI Latch Timing Diagram Including FET Coarse Bias

Processor Board 5 Volt Supplies

The amplifier's 5 volt supplies are physically located on the Processor Board. The source of the supply is the 10–volt secondary of transformer T1 in the AC Switching Module. Three DC supplies, the +5V supply, the –5V supply, and the +UNREG supply, are generated on–board the Processor Board.

The +UNREG supply derives directly from the rectifier bridge output (BR1) where a voltage of about 12 volts exists. This voltage is resistor divided down to about 4 volts where it actually becomes the +UNREG signal. Since this voltage is unregulated, the precise voltage level is proportional to the AC line voltage. The microprocessor monitors this voltage through one of the A/D inputs (U41, pin 2) and forces a fault if the line voltage goes too low or high. Table 2–2 provides a complete listing of A/D sampling and fault limits.

The +5V supply also originates from the 10VAC transformer, but is regulated through U51. This supply is used to drive Vcc, Vdd, etc.. to most logic chips throughout the amplifier. The voltage is monitored through a 2.5 volt precision reference (D3) circuit which is tied to the microprocessor reset pin (RST). The circuit–forces a reset if the +5V supply goes below approximately 4.0 volts; built–in hysteresis restricts coming back out of reset until the voltage recovers to approximately 4.5 volts.

The –5V supply is also a regulated supply (VR1) from the negative side of the rectifier bridge BR1. This supply is used to drive Vee, Vss, etc.. to logic chips such as the RS–232 drivera (U14), and provides the negative voltage supply for several opamps throughout the amplifier.

Section 2.2 Microprocessor Controller (Continued)

RS–232, SCM, PCM, and RF MON Connectors

Serial communications (RS232, J2204 connector) is accomplished through the microprocessor SCI communications bus. It is a full duplex asynchronous interface TxD at pin PD1 and RxD at pin PD0) driven by U14. This amplifier is configured through the microprocessor control registers for serial communications at 9600 baud, 1 start bit, 8 data bits, and 1 stop bit. See Chapter 3 for details of available commands and data read codes for this amplifier.

NOTE:

EPROM code defaults the BAUD register to 1200 baud should the control register be altered. This protection feature eliminates the possibility of an inaccessible SCI bus due to an unknown baud rate.

General Electric's SCM communications (SCM J2201 connector) are also handled on the Processor Board. SCM communication with the microprocessor is accomplished through the use of a 256 byte dual port RAM chip (U18). This device permits time sharing of the 8 least significant bits of the Processor Board address bus for transfer of SCM data. These same 8 bits of the address bus are also used throughout the rest of the amplifier for logic control lines. See the Motorola technical manuals and GE's technical manuals on SCM communications for details of handshaking and data transfer protocols. Some details of valid SCM read and write procedures including a timing diagram may also be found in Chapter 3.

The PCM port (P2203 connector) is dedicated to providing the UNBLANK (amplify enable) logic which gates ON the RF paths in the amplifier. This port combined with the RF MON port provide a high integrity safety system to ensure that RF is not gated on unless it is intended. Should the RF MON connector or wiring become opened or shorted, a 12 volt safety relay will lose power (supplied by RF MON) and force the amplifier into an OFF mode. The RF MON contains a pair of UNBLK logic lines which must agree with the PCM UNBLANK logic lines for the the unblank to be accepted and implemented. Two pairs of RFLCK logic lines also exist in the RF MON port which must remain correctly set to maintain the "unlock" on the gate.

Amplifier Power Supply Control

There are nine power supplies monitored by the microprocessor. The monitoring is done in most cases through a scale down resistor divider network and sampled by an A/D converter on–board the microprocessor. These resistor dividera are all made with high–impedance precision (1%) resistors. See Chapter 3 for method of reading the A/D values associated with each power supply, and for a table of associated fault codes. Table 2–2 at the end of this Section describes the A/D conversion levels and fault limits.

Three of the monitored power supplies are found on the Processor Board as just discussed. The +5V supply is actually monitored directly through the 2.5 volt reference with no conversion necessary. The –5V supply is converted to a nominal 1.7 volts using a resistor network in conjunction with the +5V supply. The +UNREG has a nominal value of about 4.5 volts and is used directly to indicate a low line voltage.

Section 2.2 Microprocessor Controller (Continued)

Four power supplies on the Power Control Board are monitored by the microprocessor. The +32 volt supply is nominally 3.2 volts after a resistor divider (R13 and R14) located on the Processor Board. The 32 volt rail is the highest voltage present on the Processor Board. The regulated +24 volt supply is also monitored on the Processor Board in the same manner (R54 and R55) at a value of 4.0 volts. The regulated +48 volt supply is resistor divided on the Power Control Board, and a value of 2.5 volts is sampled by the A/D converter at pin 4 of U45. The unregulated +100 volt bus is also sampled from a resistor divider on the Power Control Board at a nominal level of 3.2 volts.

The final two power supplies to be sampled are located on the High Voltage Rectifier/Filter Board. These are the +3KV (IPA HV and +6KV (PA HV supplies for the anodes of the vacuum tubes. Sampling of these voltages is done through a long resistor divider network located on the HV Rectifier/Filter Board which brings the sample voltage down to about 4 volts.

These two power supplies are also unique in that they turn on in two stages. The microprocessor controlled sequence of turn–on is to engage the soft start relay for about six seconds, and then engage the full run relay. See Section 2.3 for more information. The sampling of these supplies is done throughout the turn–on sequence. If the sampled values fall below a defined threshold curve in the first six seconds, a soft start fault will be issued. After soft start is complete, these supplies are handled in the same way as the other supplies.

Tube Bias and Control

The operating points for the two vacuum tubes have been chosen to optimize operation in each mode. The idle DC plate bias current for each tube in each mode (only 3CPX800A7 tube is on in HEAD mode) is set to a target value by the microprocessor. This is accomplished through current sensing resistors (R1 and R88) on the High Voltage Rectifier/Filter Board which create a voltage proportional to the plate currents of each tube. The current signals (PA and IPA I MON +/–) are transduced through opamps (U39 and U40) on the Processor Board from a differential voltage to a proportional voltage (PA and IPA PLATE I) with respect to ground for the microprocessor to sample. The microprocessor A/D converter sees a voltage equal to 0.502 times the PA (YC156) plate current and 1.968 times the IPA (3CPX800A7) plate current.

The target plate bias currents are set by the microprocessor just before going to OPERATE, and are not adjusted again once in OPERATE. The bias currents are controlled by fine voltage adjustments through DAC circuits (U23, RP7, U42 for IPA BIAS REF, and U24, RP8, and U43 for PA BIAS REF) which finely adjust the voltage applied to the cathode of each tube. The target idle plate currents for each tube (IPATARG and PATARG) in each mode are stored in EEPROM. Refer to Chapter 3 for additional information concerning memory locations.

Section 2.2 Microprocessor Controller (Continued)

The tube heater currents are also monitored on each tube (PA HTR I MON and IPA HTR I MON) to verify proper heater element operation. The grid currents present on each tube are monitored (PA GRID I MON and IPA GRID I MON) to detect large or negative grid currents which indicate a problem for the amplifier's grounded grid configuration (ideally, grld currents are near zero). Also monitored are the cathode bias voltages (PAV BIAS MON and IPA V BIAS MON) used to obtain target plate currents for each tube. See Section 2.3, *Power Supplies* for further information.

FET Bias and Control

The amplifier employs a method similar to the tube biasing for setting and maintaining the DC bias currents of the RF field effect transistors (FETs) on the Solid State Amplifier Board. The FETs are biased to an optimum operating point for each stage. Fluctuation of this bias would affect performance; therefore, the microprocessor periodically checks and finely adjusts the bias to maintain the ideal level. This is accomplished during periods of STANDBY mode and OPERATE mode with no UNBLANK present. See also Section 2.1.1 for a discussion of the FET biasing.

The first step in the bias method may be termed the "ballpark" routine. This procedure is executed immediately prior to going to STANDBY. The routine consists of presetting each of the Processor Board "fine" DAC circuits (U35–U36, RP9–RP12, and U47–U50) one at a time to a value sufficient to turn on the FETs (see Section 2.1. 1). The corresponding coarse DAC on the Solid State Amplifier Board (U6) is then adjusted to produce a "ballpark" bias current just above the target value. The amplifier then proceeds to the STANDBY mode where "Dynamic Refresh" is enabled to adjust the Processor Board fine DAC circuits to bring the individual FETs to the desired bias current and maintain them there in both STANDBY and OPERATE modes.

During the ballpark routine, the coarse DAC is driven in a ramp (100 microsecond steps) from 0 to 5 volts maximum for each FET. The DAC has 6 bit resolution yielding 78 millivolt (ideal) incremental steps. The DAC is a very non–linear 6–bit device, and actual single–bit resolution can be anywhere from 19 to 137 millivolts per step. The adjustment algorithm is executed for FET 1 through FET 4 whether or not previous target biasing for an FET has failed. Therefore, a fault (if any) indicates the last FET that failed the ballpark algorithm. For example, if an FET 1 fault is indicated, then FETs 2 through 4 must have passed. The four DACs are assigned in the order DAC output 1 = FET 1 = Q26 (MRF148, outside), DAC output 2 = FET 2 = Q25 (MRF148, inside), FET 3 = Q28 (MRF150, outside), and FET 4 = Q27 (MRF150, inside).

The fine DAC circuits are 8 bits wide (256 steps) and are used to vary the gain of the bias control opamps on the Solid State Amplifier Board. The total adjustment range of the fine DAC is equal to about 5 bits of the coarse DAC. The net adjustment effect of the fine DACs is to subtract a small voltage from the gates of the FETs. Therefore, the ballpark routine adjusts the coarse DACs to the first step above the target bias current. The initial convergence algorithm for the fine DACs starts when the amplifier reaches STANDBY and should be stable about 10 to 20 seconds later.

Section 2.2 Microprocessor Controller (Continued)

Amplifier Tuning and AFT

Each amplifier is tuned to its optimum operating point before leaving the factory. The factory tune–up adjusts three resonant tank circuits, IPA input from the Solid State Amplifier, the IPA output, and the PA output, used for impedance matching between stages and the external world. Each of these tuned circuits consists primarily of a pi–tank circuit using shunt tune and load capacitors separated by an inductor.

The object of the IPA input tank is to impedance match the IPA stage to the Solid State Amplifier Board so that minimal power is reflected back into the Solid State Amp. This tune is done by hand, and is totally unrelated to the Processor board. (Refer to Sections 2.1.1 and 2.1.2 for details about this adjustment.)

The IPA and PA output tanks are entirely under microprocessor control. These circuits are implemented with stepper motors on the tune and load capacitors. The circuits are dynamic to allow for adjustment against small production variations in the field replaceable YC156 and 3CPX800A7 tubes. Additionally, the IPA output tank circuit must be able to switch between the 50 ohm HEAD mode and the input to the PA stage.

The primary purpose of the automatic fine tuning (AFT) algorithm is field replacement of tubes (both YC156 and 3CPX800A7). AFT of a given stage consists of adjusting the appropriate “tune” capacitor (motor 1 for IPA or motor 3 for PA) until a null is achieved as measured by the corresponding phase detector (“null” is 2.5 volts as seen by the microprocessor). The tuning capacitors are used to adjust for variation in the reactive components in the circuit (particularly in replacement tubes) by zeroing the phase difference between the cathode and plate. Zero phase indicates that an optimal resistive load has been achieved. The load motor (and capacitor) positions are fixed once they leave the factory, and will not be moved during AFT. They only move to assigned positions for mode changes. Refer to the Section 2.1.2 for more details.

The AFT routine can be enabled or disabled using the serial command set. If AFT is enabled, then it will occur whenever the amp is brought from STANDBY to OPERATE regardless of whether or not a mode change has occurred previously. The serial commands “A+” and “A–” enable and disable AFT respectively. These commands are presented in Chapter 3, Section 3.2 with the rest of the serial and SCM commands.

The BODY mode AFT sequence is tune IPA, tune PA, tune IPA, tune PA, and OPERATE. Head mode AFT consists of tune IPA, and OPERATE.

Motor Control

As mentioned above, the stepper motors are used by the microprocessor to adjust the amplifier’s tune through the AFT algorithm and factory tune–up. The numerical ordering of the motors starts at the bottom with #1, and consecutively counts up with the top motor being #4. Table 2–1 provides a summary of the motor implementation.

Section 2.2 Microprocessor Controller (Continued)

Table 2–1 Motor Implementation

Motor	Capacitor Type	Steps/Gearing
#1	air variable	900 steps (9:1 gear reduction)
#2	air variable	100 steps (direct drive)
#3	vacuum variable	3400 steps (direct drive)
#4	vacuum variable	3400 steps (direct drive)

The motors are 6–lead variable reluctance and permanent magnet hybrids with 200 steps per full turn of the motor shaft. The motor drives consist of four “phases” (two center–tapped coils tied to +32 volts at center) used to single–step the shaft. Motor phases are driven by sequentially lowering the ends of the coils through driver chips U21 and U22. Only one half–coil is energized at a time. For example, motor 1 coil ends are labeled 1A, –1A for coil 1, and 2A, –2A for coil 2. Suppose the motor is resting at a step such that –1A and –2A are energized (1A and 2A are open). A step of the motor maybe obtained by first raising –1A (so that now only –2A is energized; this is called a half–step), and then lowering 1A so that 1A and –2A are now energized. The next sequential step consists of first raising –2A, and then lowering 2A so that 1A and 2A are then energized. When the fourth sequential step is taken, the coils are back to the state with 1A, –2A energized ana 1A, 2A open.

The microcontroller sets the “tuned” motor positions by first finding the “zero” position (occurs during OFF to STANDBY. Zero is defined by an optical sensor mounted on the motor assembly. The motors are turned to the desired destination a defined number of steps away from zero. The proper number of steps for each motor in each mode is stored in microprocessor memory.

The motors can also be independently turned to any location while the amplifier is in OFF using the serial ‘T’ command as discussed in Chapter 3. An attempt to turn a motor past its maximum will result in banging the motor into its hardware limit. Although the sound of this effect is rather harsh, it should not damage any of the hardware. It should be avoided, however, since the shaft couplings might slip leaving the amplifier mistuned due to error in the zero location.

Fault Testing and Overall Amplifier Monitoring:

The entire amplifier is thoroughly monitored by the microprocessor through A/D conversions and transducers such as those mentioned for the power supplies earlier in this Section. The purpose of the monitoring process is to detect irregularities that may affect the operation of the amplifier. The data is also quite useful for diagnostic purposes as described in Chapter 4.

Section 2.2 Microprocessor Controller (Continued)

There are 32 analog test points within the amplifier that are sampled by the microprocessor. These samples are read–only, and generally are obtained by eight microprocessor A/D channels and four multiplexers. Table 2–2 at the end of this Section describes each of these test points including the fault limits associated with the fault codes in Chapter 4 and the digital conversion from bits (0–255 decimal, 00–FF hex) to real data. Real data may be obtained from the binary bit value by noting that 256 bits is full scale 5 volts and is used for all A/D conversions; the bit resolution is 0.0195 volts per bit. Thus a conversion unit obtained from Table 2–2 may be converted to several equivalents. For example, the “SS Amp FET Bias” has a digital conversion of 5 mA per bit. This is the same as 256 mA per volt, or 0.004 volts per mA of FET current are obtained at the current transducer by the A/D converter. All of the analog samples may be read over the SCM and serial interfaces as described in Chapter 3. The PA and IPA forward powers, PA and IPA reflected powers, PA and IPA grid currents, and PA and IPA plate currents are sampled every 500 microseconds only when the amplifier is in OPERATE. All other A/D samples are made on the order of every three to four milliseconds.

Absolute Addressing

In Chapter 3, Table 3–10 contains two bytes (4C and 4D) that may be used to determine the absolute microprocessor address of any of the RAM codes in the table. This feature is provided because the base address of the table is dynamic with respect to software revisions. Under special circumstances it may be desirable to be able to write data to one of these addresses. This must be done over the serial bus using the serial commands detailed in Chapter 3.

WARNING:

Do not attempt to write data to microprocessor addresses other than those specifically prescribed by documented procedures. Writing data to microprocessor addresses can be extremely hazardous to the amplifier and associated personnel.

The data in 4Ch and 4Dh is called the SCMTABLE where 4D is the least significant byte, and 4C is the most significant byte. The equation below is used to determine the absolute address of any code:

absolute address = 256 x (value at entry_addr+0) + (value at entry_addr+1)
where entry_addr = SCMTABLE + 2 x code

The number 256 is decimal; use 100h if doing multiplication in hexadecimal. For example, suppose it is desired to find the absolute address of FET3,4 Bias Target (address code 01h). Address codes 4C and 4D yield C3h and 29h respectively. Therefore, SCMTABLE is C329h (49961 decimal), and entry_addr is C32Bh (49963 decimal). The contents of entry_addr and entry_addr+1 are read over the serial port and found to be 30h and 82h respectively (48 and 130 decimal). Therefore, the absolute address of FET3,4 Bias Target is 100h x 30h + 82h = 3082h (256 x 48 + 130 = 12418 decimal).

Section 2.2 Microprocessor Controller

Table 2.2 Analog Test Points

Code	Signal	Digital Conversion	Fault Limits: Low / (High)
00h	IPA Forward Pwr	0.049 volts/bit, where KWatts = (volts^2)/50	none / (2.52 KW HEAD) (203 W BODY)
01h	IPA Grid Current–	4 mA/bit	none / (324 mA.)
02h	IPA CATHODE Bias	0.16 volts/bit	none / (30.2 volts)
03h	Unused (reserved)	N/A	N/A
04h	IPA Plate Current	9.96 mA/bit	none / (none)
05h	SS Amp Heat Sink	none	25 deg. F/(140 deg. F)
06h	+UNREG	0.061 volts/bit	9.27 volts /(14.64 volts)
07h	PA Tune	0.0196 volts/bit, where where (Phase Detect)	0.18 volts / (4.84 volts) in phase = 2.5 volts
08h	PA Forward Pwr	0.155 volts/bit, where: KWatts = (volts^2)/50	none / (39 W HEAD) (23.47 KW BODY)
09h	PA Grid Current	4 mA/bit	none / (564mA)
0Ah	PA Cathode Bias	0.48 volts/bit	none / (101.8 volts)
0Bh	Fan Air 2	none	0 bits / (255 bits)
0Ch	PA Plate Current	39.09 mA/bit	none / (none)
0Dh	SCM Interlock	none	none / (129 bits)
0Eh	IPA Tune	0.0196 volts/bit, where (Phase Detect)	0.18 volts/(4.84 volts) in phase = 2.5 volts
0Fh	100 Volt Supply	0.613 volts/bit	87.7 volts / (147 volts)
10h	IPA Reflect Pwr	0.049 volts/bit, where KWatts = (volts^2)/50	none / (1.3 KW HEAD) (209 W BODY)
12h	IPA Heater Current	19.6 mA/bit	1.16 Amps / (1.88 Amps)
13h	IPA Envelope	none	none / (none)
14h	–5 Volt Supply	(–0.058) volts/bit	–4.23 volts / (–5.39 volts)
15h	Motor Drive 1	none	0 bits / (none)
16h	SS Amp FET Bias	5.00 mA/bit	none / (none)
17h	+48 Volt Supply	0.376 volts/bit	42.9 volts / (51.5 volts)
18h	PA Reflect Pwr	0.155 voltsibit,where KWatts = (volts^2)/50	none / (48 W HEAD) (12.9 KW BODY)
19h	+6 KV Supply	31.9 volts/bit	4500 volts / (7592 volts)
1Ah	PA Heater Current	196 mA/bit	10.6 Amps / (18.6 Amps)
1Bh	Tube Air 2	none	0 bits / (255 bits)
1Ch	+32 Volt Supply	0.196 volts/bit	21.8 volts / (38.4 volts)
1Dh	motor drive 2	none	0 bits / (none)
1Eh	+5 Volt (2.5 Volt)	0.0196 volts/bit	2.23 volts / (2.67 volts)
1Fh	+24 volt supply	0.117 volts/bit	20.94 volts / (25.04 volts)

Section 2.3 Power Supplies

The Erbtec MRI amplifier uses several varieties of power supplies within the amplifier. Supplies are designed around the particular needs of a circuit or group of circuits to be powered. The discussion of these supplies is divided into subsections with respect to where the supplies are located in the amplifier. The primary power supplies discussed in this Section are on the Processor Board, the Power Control Board, and the High Voltage Rectifier/Filter Board.

A simplified functional block diagram of the power supplies and their locations is provided in Figure 2–6 below. Table 3–3 at the end of this Chapter summarizes the power supply distribution and utilization.

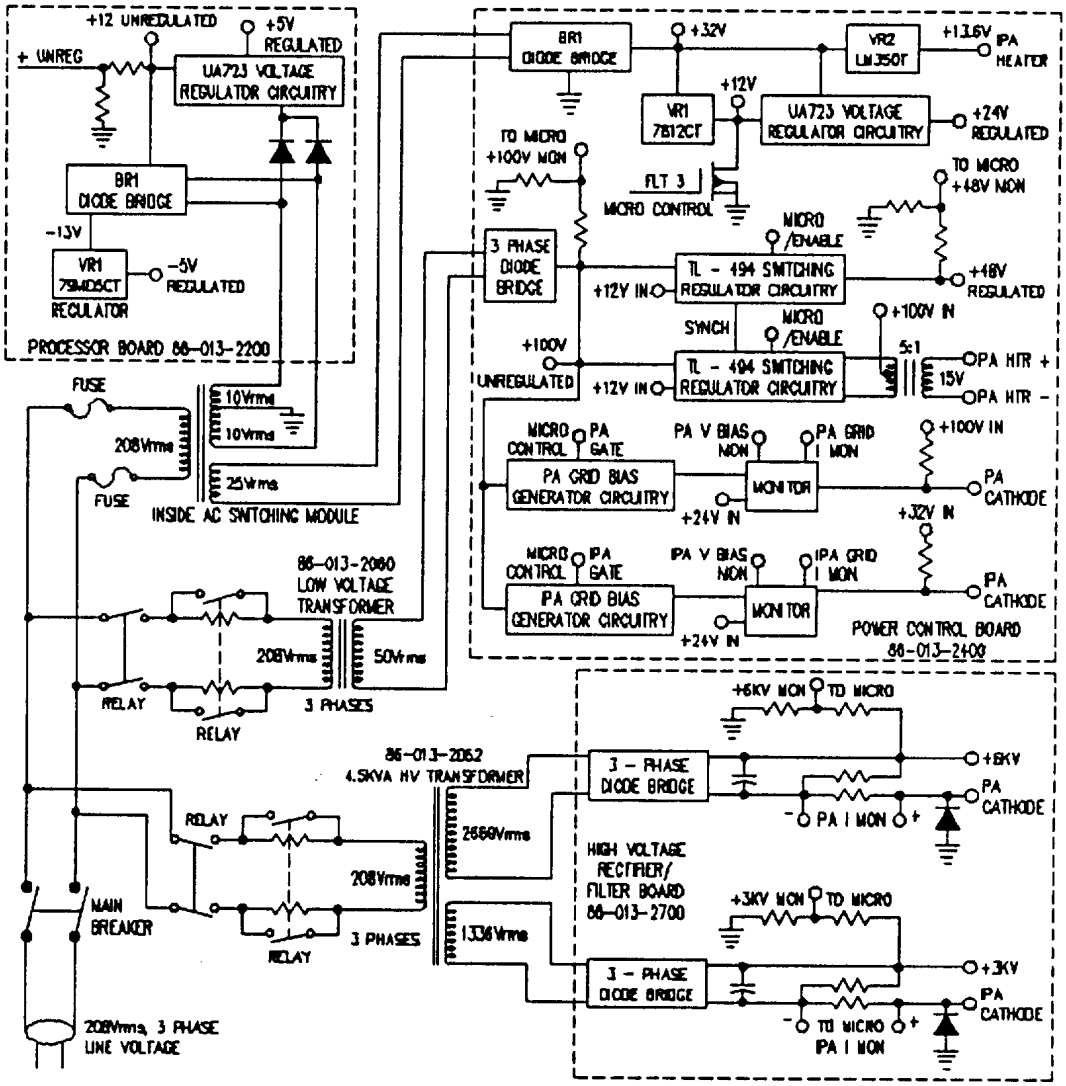

Figure 2–6 Functional Block Diagram of Amplifier Power Supplies

Section 2.3.1 Processor Board Power Supplies

Overview

There are two regulated power supplies that reside on the Processor Board (see schematic 86–013–2210). The primary +5 volt supply exists on this board to power all the microprocessor logic circuitry as well as much of the rest of the amplifier's logic circuitry. The Processor Board also contains –5 volt supply for the many components requiring a negative rail such as some operational amplifiers. Both of these supplies are regulated, and are derived from a center–tapped 20 Vrms transformer secondary located in the AC Switching Module. The microprocessor also makes use of the unregulated voltage before it becomes regulated as described in the +UNREG section below.

+UNREG

Both of the 5 volt supplies receive their power from the single–phase transformer (T1) located in the AC Switching Module (schematic 86–013–21 10). A 20 Vrms center– tapped winding is dedicated to these supplies. Fuses F1 and F2 in the AC Switching Module protect the transformer against wiring or component failures. Bridge rectifier BR1 on the Processor Board converts the transformer voltages to unregulated DC, and two capacitors filter the voltage for use by their respective regulatora. Capacitor C132 is the storage capacitor for the unregulated + 12 volts, and C106 is storage for the –12 volt side. The +5 volt regulator (U51) also uses a small control–voltage supply drawing additional energy from the transformer winding through diodes D14 and D15, and uses capacitor C1 14 for filtering and storage.

Then unregulated + 12 volts is used by the microprocessor to determine if the input line voltage has fallen below 187 Vrms. The 12 volts is resistor divided down to 4 volts so that the 5 volt A/D channels in the microprocessor can monitor it.

+ 5 Volt Regulator

The +5 volt regulator is a linear type utilizing active voltage regulation and foldback current limiting above 2 Amps output current. An output protection zener (D16) ensures that an externally supplied voltage, either positive or negative, will be clamped at a safe level to protect the regulator and its load circuitry.

The +5 volt supply is controlled by a uA–723 regulator integrated circuit (U51) which houses a voltage reference, voltage error amplifier, current limit sense circuitry, and the drive amplifier for an external regulator transistor. The heat sunk TIP–100 regulator transistor (Q3) is the actual supply control element which maintains the output voltage constant.

The voltage adjustment R122 allows for accurate setting of the desired operating voltage, and is set to exactly 5.00 volts at the factory. Accuracy is important since it is also used by the A/D converter (on–board microprocessor) as the reference voltage. Resistor R98 is used to sense the supply's output current, and makes up part of the foldback current–limiting circuitry.

Section 2.3.1 Processor Board Power Supplies (Continued)

The 5 volt uA–723 regulator circuit requires a control supply voltage of at least 9 volts to operate properly. It receives this voltage from C114. The main power supply receives its power from C132 and can be regulated properly with the C132 voltage down to a little below 7 volts. During a power–down event (loss of line power or circuit breaker trip), the +5 volt supply can maintain regulation for about 100 ms. During this time the microprocessor senses the falling voltage on C132, and stores vital data into its EEPROM memory. The control power voltage on C114 does not drop below 9 volts during this critical time.

–5 Volt Regulator

A three terminal, non–adjustable 79M05CT regulator (VR1) is used for the –5 volt supply. VR1 has internal current limiting and over–temperature shutdown circuitry. The output voltage is not adjustable, but the rated 10% range is acceptable in this application. Printed circuit board ground–plane copper is used to provide a sufficient heat sink for its operation.

Section 2.3.2 Power Control Board Power Supplies

Overview

The Power Control Board (schematic set 86–013–2410) contains a number of power supplies, voltage regulators, and the tube bias control circuitry. The Power Control Board is the primary source of most of the required amplifier supply voltages with the exception of tube anode voltages and the 5 volt supplies. Main power is supplied to the Power Control Board from transformer T1 in the AC Switching Module, and from the 3–phase Low Voltage Transformer mounted next to the Power Control Board.

+32 Volt Unregulated Supply

The +32 volt unregulated power supply circuitry receives its power from a 25 Vrms winding on the single–phase transformer T1 located in the AC Switching Module (schematic B6–013–2110). Primary winding fuses F3 and F6 protect the transformer against wiring or component failures. Bridge rectifier BR1 on the Power Control Board converts the transformer voltage to DC, and capacitor C52 filters the raw DC for use by the loads utilizing this voltage.

The +32 volt supply is powered up whenever the amplifier is supplied with main power and the circuit breaker CB1 on the rear panel is ON. This supply has a 3.5 amp capability, and is used for stepping motor excitation, +12 volt supply regulator power, +24 volt supply regulator power, and the IPA tube heater supply regulator power.

Section 2.3.2 Power Control Board Power Supplies (Continued)

+12 Volt Control Power Supply

The +12 volt control power supply is utilized only by the other regulator circuitry on the Power Control Board. A three terminal non–adjustable 7812CT regulator VR1) is used for the supply. Absolute voltage is not critical since the integrated circuits utilized are designed to operate over a large range of voltages. This supply is entirely dedicated to ensure that all internal control circuitry utilized for power supply control will not be disrupted by external faults on the other regulated supply busses. Diode D33 also protects the VR1 regulator from reverse voltages in case of a short on the +32 volt bus which sources the +12 volt supply.

+24 Volt Regulator

The +24 volt regulator circuitry is a linear type regulator utilizing active voltage regulation and foldback current limiting above 2 amps of output current. The supply is controlled by a uA–723 integrated circuit (U10) which houses a voltage reference, voltage error amplifier, current limit circuitry, and the drive amplifier for an external regulator transistor. The heat–sink TIP–145 regulator transistor (Q27) receives its power from the +32 volt bus, and is the actual supply control element which maintains the output voltage constant. Operational amplifier U9 performs the foldback current control.

Control resistor R92 sets the voltage regulation level of the supply, and control resistor R84 sets the foldback current level to 2 amps for full output. The +24 volt regulator is shut down by the microprocessor if the supply becomes unregulated by setting the “FLT 3” line low (see Table 2–2, Section 2.2 for fault limits). Diode D32 protects the regulator circuitry against reverse voltages if the +32 volt bus is faulted. The +24 volt supply is used for biasing the MRF134 FETs on the Solid State Amplifier Board, driving the relay coils in the AC Switching Module, the RF Monitor Module, and the PA Input Board, and supplying the positive rail for several op–amp circuits throughout the amplifier.

+100 Volt Unregulated Supply

The +100 volt unregulated power supply receives its power from three 50 Vrms windings in the three–phase “delta–wye” Low Voltage Transformer (86–013–2060) located on the inside of the rear amplifier panel (86–013–0503). Primary winding fuses F10, F11, and F12 (located in the AC Switching module) protect the transformer against wiring or component failures. The bridge rectifier formed by D26 through D31 converts the three–phase transformer voltage to DC, and capacitor C48 filters the raw DC for use by the loads.

The +100 volt supply is powered up whenever the amplifier is in any mode other than OFF (supply is on when the fans and blower are running). This supply has 3 amp capability, and is used for PA blanking grid bias, PA and IPA grid bias generators, the +48 volt supply regulator power, and the PA heater regulator power.

Section 2.3.2 Power Control Board Power Supplies (Continued)

+48 Volt Regulator

The +48 volt supply is a single inductor switching regulator utilizing active voltage regulation and protective current limiting set at about 2.5 amps. It receives its power from the +100 volt unregulated power supply. The supply is controlled by a TL–494 switching regulator integrated circuit (U1) which houses a voltage reference, voltage error amplifier, current limit circuitry, and pulse width modulator. The heat–sink IRF9641 FET power switch (Q2) receives its drive from U1 via voltage translator Q7 and a floating emitter follower drive circuit utilizing Q3 and Q4. L1 is the energy storage inductor; C14 is the energy storage capacitor, and D2 is the flywheel diode (supplying current when Q2 switches off. R1 is used as a current sensing shunt for the protective current limiting circuit using Q1 as a level translator.

Control resistor R10 allows the supply voltage to be accurately set at +48 volts. The current limit is not adjustable since its absolute level is not critical. The regulator is turned on and off with the “/ENABLE” signal driving Q8 when set by the microprocessor controlled “HTR ENABLE” line which simultaneously turns on the tube heaters. When the regulator is commanded on, it soft starts while capacitor C19 charges up.

The internal clock oscillator in the TL–494 runs at 50 to 60 KHz, and is used as a “SYNC” signal for the PA tube heater supply (also a TL–494) operating from the same clock to avoid any beat frequency problems.

The +48 volt supply is used for the Class AB FET amplifier stages (MRF 148s and MRF 150s) on the Solid State Amplifier Board. The 50,000 microfarad Aluminum Electrolytic Capacitor (125–4125) is placed across the +48 volt bus to supply the large pulse–currents required by the Solid State Amplifier Board.

PA Heater Regulator

The PA tube heater supply is a push–pull transformer–coupled switching regulator utilizing active voltage regulation and protective current limiting set at around 18 amps. It receives its power from the +100 volt unregulated power supply. Transformer coupling allows the supply output to float with respect to ground for use by the PA tube grid bias. The PA tube cathode (tied to unregulated + 100 volt supply) and heater are tied together which requires the heater to be able to float at the cathode potential.

The TL–494 switching regulator integrated circuit (U2) is the same IC as that used for the +48 volt supply; it contains a voltage reference, voltage and current feedback amplifiers, a pulse width modulator and switch transistor drive circuits. Voltage sensing is done by an error amplifier circuit that floats on the supplies output. Operational amplifier U4 senses the supply output voltage and compares it against a reference zener diode D14. The drive signal is transmitted to the TL–494 through an optical isolator U3. Control resistor R41 sets the comparison level for the operational amplifier.

Section 2.3.2 Power Control Board Power Supplies (Continued)

The power switching FETs (Q5 and Q6) receive their gate drives from U2 via drivers Q9 and 010. Zener diodes D35 and D36 help protect the high impedance gates of the FETs. Q5 and Q6 drive the 5:1 step–down transformer T1 matching the 100 volt source to the 15 volt load and providing five times more current. Protective current limiting for the supply is performed by sensing the currents in the switching FETs using R14, R15, D7, R37, R38, R39, and reducing the switching duty–cycle if the currents go too high.

Diodes D8 and D9 rectify the output of T1, and C10 filters the waveform into DC. Filter transformer T2 and capacitors C11, C12 and C65 eliminate the switching transients that can effect the amplified RF signal coming through the PA tube. The “/ENABLE” signal through Q11 turns the regulator on which then soft starts as capacitor C23 charges up.

IPA Heater Regulator

The IPA tube heater supply is a linear regulator circuit powered through the +32 volt unregulated supply and a LM350T adjustable regulator VR2). The IPA tube heater is isolated, so it is a fairly constant load and does not require a floating supply as the PA heater does. The resistance does vary considerably with warm–up time, but once the six minute STANDBY to OPERATE cycle is finished, the resistance remains fairly constant.

The LM350T is set to 15.2 volts (value at the Power Control Board output only; about 13.6 volts at the tube heater) through control resistor R108. Power transistor T1P105 (Q29) provides the bulk of the heater current through resistors R106 and R107. The current is made variable by tying the LM350 to Q29 through R105. This feature also limits the current allowed into the tube heater at initial turn–on.

The IPA tube heater supply is turned on and off by the “/ENABLE” and “HTR ENABLE” lines through Q12 and Q28. The heater is regulated in the sense that the microprocessor monitors the current and issues a fault if the current falls out of acceptable range (see Table 2–2, Section 2.2).

Vacuum Tube Grid Bias Generators

Both the IPA and PA vacuum tube stages have grid voltage (actually applied to cathode) bias generators that allow the microprocessor to Set the BLANK (idle) plate currents to predetermined values. This freedom automatically compensates for changes in plate voltages and the different operating points of different tubes. This circuitry resides on the Power Control Board, and the IPA stage generator is identical to PA stage generator except for a few minor details. For this discussion the PA grid bias generator section is described, and differences of the IPA are discussed as applicable.

The bias generator is made of two separate functional parts, a bias reference supply and a bias switch, which have their circuitry integrated together. The bias reference supply generates a voltage that the tube grid is connected to when it is active. The bias switch itself does the connecting to the tube. Both the IPA and PA tubes are operated in hard grounded grid; therefore, the grid bias must be applied in the opposite potential to the cathode.

Section 2.3.2 Power Control Board Power Supplies (Continued)

The shunt regulated bias reference supply is programmed from the microprocessor by one of its 0 to 20 volt DAC outputs. Charging current is supplied to a storage capacitor C39 from the +100 volt bus. The current flows through R50 and zener diode D20. The zener provides a floating supply to power the bias switch. Power FET Q23 shunts current from the capacitor and discharges it to a desired value. Operational amplifier U8 compares the capacitor voltage with the DAC voltage and drives the FET gate to correct for errors. The IPA bias supply tracks the DAC directly, and the PA bias supply multiplies the DAC voltage by 150% with the R65–R66 voltage divider.

The bias switch floats on top of the storage capacitor C39 and receives its UNBLANK commands through the opto–isolator U6. Transistors Q17, Q18, and Q19 provide the required drive to the power FET switch used to pull the cathode voltage down from its BLANK level. The PA cathode is referenced to the +100 volt bus during blanking by R82. The IPA cathode is pulled up to the +32 volt bus by R81. An emitter follower Q25 is used to pull the cathode line down, and passes the tube grid currents through its collector lead to shunt resistor R78 where the microprocessor can monitor it. Zener diode D21 (in the PA switch only) generates an additional bias voltage range offset needed in that stage.

Section 2.3.3 High Voltage Power Supplies

Overview

There are two high voltage power supplies, +3 kilovolts (KV), and +6 KV, in the amplifier used as anode bias voltages for the vacuum tubes. Both of these power supplies share much of the same circuitry and are located on the High Voltage Rectifier/Filter Board (schematic set 86–013–2710). The main power is supplied through the AC Switching Module (schematic set 86–013–2110) to the 4.5KVA HV Transformer (86–013–2062) and then to the High Voltage Rectifier/Filter Board. Both supplies are floating with their negative leads connected to the cathodes of their respective tubes.

Contribution of the AC Switching Modules

Closing relay K3 in the AC Switching Module “soft–starts” the three phase 208 Vrms excitation to the primaries of the 4.5 KVA HV Transformer through resistors R1 and R2. These resistors limit the in–rush current to the transformer primary. The Low Voltage Transformer used by the +100 volt unregulated supply is also soft–started in this manner. The soft–start action allows controlled charging of the +3 KV and +6 KV filter capacitors (C1–C8 for +3 KV and C1 1–C26 for the +6 KV on the High Voltage Rectifier/Filter Board. After a few seconds time, the capacitor voltage reaches a value where it is safe to apply full line voltage to the supply. Relay K4 in the AC Switching Module (or solid state relays SW1 and SW2 in AC Switching Module 2) is commanded to close thus bypassing the two soft–start resistors.

Circuit breaker CB1 provides current–limit (15 amps per phase) protection to the high voltage supplies.

Section 2.3.3 High Voltage Power Supplies (Continued)

There is a fast shutdown arc detection circuit on Processor Board which will quickly open relays K3 and K4 in the event of a high voltage arc. A high voltage arc suddenly puts the +3 KV or +6 KV lines to ground which is equivalent to the cathode side of the floating supply being at –3 KV or 6 KV with respect to ground. This causes transistor Q2 on the Processor Board to turn on through either D10 or D11 and the respective signals “PA I MON–” and “IPA I MON–” which then lowers the PA7 interrupt line. This interrupt immediately prompts the microprocessor to open K3 and K4.

High Voltage Transformer

The 4.5KVA HV Transformer is a three phase “delta–wye” shielded transformer designed to operate from a 208 Vrms line to line voltage without a neutral connection (“delta”primary). Electrostatic and corona shields have been provided for protection and low noise operation.

Each of the high voltage supplies (+3 KV and +6 KV have separate floating “wye” connected secondaries. The secondary winding leads are constructed to plug directly onto the HV Rectifier/Filter Board for ease of installation.

High Voltage Rectifier/Filter Board

The +6 KV circuitry uses high voltage diodes D19 through D24 to rectify the three–phase secondary voltages into DC. Sixteen 450 volt filter capacitors C11 through C26 are connected in series across the supply to achieve a sufficient voltage capacity to safely hold the +6 KV. Pairs of 100 kiloohm bleeder resistors are connected across each capacitor to bleed the capacitors and to ensure that capacitor leakage currents do not unbalance the voltage division across the capacitors.

Resistor R88 is in series with the negative output lead of the supply and limits the current in the case of a tube arc. R88 is also used as a current shunt for measuring the supply output current. Resistors R76 through R87 provide isolation to a differential amplifier on the Processor Board which converts the R88 voltage to a level readable by the microprocessor. Diode D12 allows the supply to float above ground (at the YC–156 grid bias voltage), but at the same time provides a path for discharging the supply during high voltage arcs. Voltage divider resistor chain R27 through R43 scales the supply voltage for the microprocessor to monitor the +6 KV supply.

The +3 KV rectifier and filter circuitry functions in the same way as the +6 KV circuitry. Since the supply voltage is half of the +6 KV supply, it requires half of the components in the capacitor and resistor stacks. Diode D1 allows the supply to float as well as provide a discharge path for the capacitor bank during an arc. A differential amplifier is provided on the Processor Board for supply current monitoring from the voltage developed across R1 and current–isolated through R2–R5, R7, and R8. Resistors R18 through R26 scale the supply voltage for monitoring by the microprocessor.

Transient clamp diodes D2–D11 are provided to protect the microprocessor circuitry during either PA or IPA arcs.

Section 2.3 Power Supplies (Continued)

Table 2.3 Power Supply Distribution

Supply	Origin	Distribution
+5 Volts	Processor Board	Logic circuit
–5 Volts	Processor Board	Op–amps, RS–232 Drivers
+32 Volts	Power Control Board	Stepping motors, + 12 volt reg. IPA grid bias, +24 volt reg. IPA heater reg
+12 Volts	Power Control Board	+24 volt reg.. +48 volt reg.. PA and IPA heater reg.
+24 Volts	Power Control Board	MRF134 FETs, Op–amps
+100 Volts	Power Control Board	PA and IPA grid bias, PA heater reg. + 48 volt reg
+48 Volts	Power Control Board	MRF148 and MRF150 FETs
PA Heater	Power Control Board	PA tube heater
IPA Heater	Power Control Board	IPA tube heater
+3 KV	HV Rect./Filt. Board	IPA tube anode
+6 KV	HV Rect./Filt. Board	PA tube anode

CHAPTER 3 AMPLIFIER FIRMWARE

Section 3.1 Overview

This Chapter completely describes the microprocessor utilization in the amplifier. The information here includes all of the commands necessary to operate the Erbtec 86–013–0000 MRI Amplifier over General Electric's SCM data bus (SCM is defined below) or over an RS–232 serial bus. The microprocessor's addressing scheme and memory allocation are discussed in detail.

The microprocessor (68HC1 1 Microcontroller) utilizes EPROM, on–board EEPROM, and both on–board and off–board RAM. The EEPROM usage is particularly pertinent information since much of the amplifier characterization data such as FET bias targets and tube on–time is stored there. Section 3.4 explains the options available for gaining access to the stored microprocessor data.

Also included is a description of microprocessor functional chronologies in Section 4.5. This Section outlines the algorithms used by the firmware to perform all primary functions such as OFF to STANDBY and UNBLANK interrupt. The material in this Chapter will be particularly helpful in overall amplifier trouble shooting and diagnostics. Several Sections in Chapter 4 refer to portions of Chapter 3.

Section 3.2 Amplifier Command Structure

Operation of the amplifier is ordinarily handled through the SCM digital interface. This port complies with the BISYCL and BICYCLE communication links which define a set of commands and timing requirements used to control amplifier operation. A valid connection must exist at this port for the amplifier to operate with the GE SIGNA MR system.

This amplifier also has an RS–232 serial communication link which can duplicate all SCM commands. A set of "enhanced" commands also exist for this port which are intended for factory use, diagnostics, and tube replacement/retuning. Ordinary operation of the amplifier does not require the serial port to be connected.

Section 3.2.1 SCM Commands

The System Control Module (SCM) interface port P2201 must be connected at all times for the MRI amplifier to function. Primary control of the amplifier is accomplished through the SCM communication port.

SCM port communication is done through four addresses numbered 01 – 04. (Supplemental addresses also exist for monitoring the amplifier microprocessor; these are described in Section 3.5.1.) The first three addresses have both read and write latches; address 04 has only a read latch. The amplifier periodically scans the interface, reads the computer's write latch, and updates the computer read latch. The amplifier must acknowledge read and write attempts by setting the "ACK" line true (see pin description tables in Appendix A) before any read or write will occur. The timing diagram for SCM logic is detailed in Figure 3–1 below. The function and definition of each address is described on the next few pages. Table 3–1 provides a summary of the discussion at the end of Section 3.2.1.

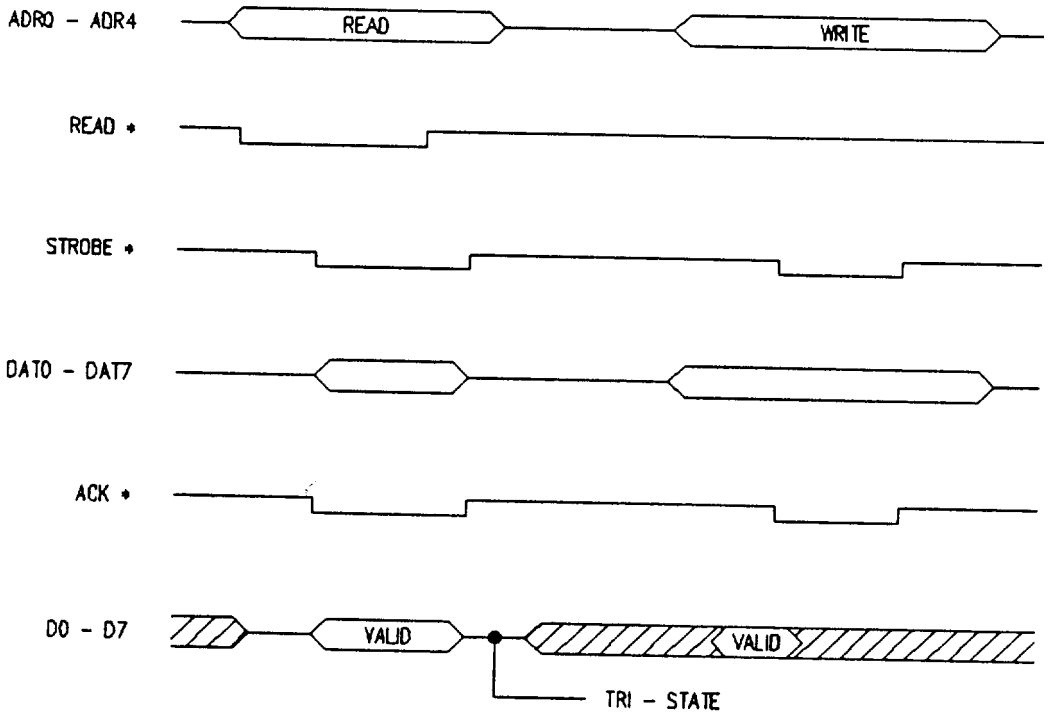

Figure 3–1 SCM Logic Timing Diagram

Section 3.2.1 SCM Commands (Continued)

Response sequence to a write at address 01

1. Byte is first echoed with none of the written changes except with the ‘Wait’ bit set.
2. Byte is echoed exactly as it is read at the port except with the ‘Wait’ bit set. This occurs within 10 milliseconds.
3. Command is executed. This could change other status bits such as the “standby’ bit.
4. If byte is remains same as in step 2, then it is echoed with ‘Wait” cleared. Other–wise,start again at step 1 to process next bit command.

NOTE;

If a byte is written to an address in which several bits change, the amplifier responds to the bit 0 change first, then the bit 1 change (if still applicable), etc.

Response sequence to a write at addresses 02 – 04

1. Status byte is returned with no changes except ‘Wait’ bit set.
2. Changed address byte is echoed within 10 milliseconds.
3. Command is executed
4. If no other address has been changed, the”status” byte is echoed with ‘Wait’ cleared. Otherwise, start again at step 1.

Address 01: “Control and Status” Byte

Write Bits:

Bit 0 is the “power off’ command when false and the ”power on” command when true.

Bit 1 is the “return to ready’ command when false and the ”goto operate” command when true.

Bits 2–7 must be written false for a command to be accepted. If any are written true, the amplifier assumes that the interconnecting cable is disconnected or broken and returns to the”power off’ state. Should this occur a “safety interlock” fault 11 is generated.

Section 3.2.1 SCM Commands (Continued)

Read Bits:

Bit 0 is the “power on” command echo. It reflects the last recognized state of the “power on/power off” command bit.

Bit 1 is the “goto operate” command echo. It reflects the last recognized state of the “goto operate/return to ready” command bit.

Bit 2 is the‘Wait’ status echo. True indicates that a command is being executed and there is a delay in progress. False indicates the amplifier is not currently processing a command and is ready to receive a command.

Bit 3 is the STANDBY mode echo. True indicates that the amplifier is in the STAND-BY mode with high voltage on to the tubes. False indicates that the amplifier is not in a STANDBY mode; the tube warm–up delay is not yet complete.

Bit 4 is the OPERATE mode echo. True means that a “goto operate” command has been successfully completed, and the amplifier is ready for RF drive. False indicates that the amplifier is not ready to amplify RF drive.

Bit 5 is the microprocessor ‘Watchdog” echo. False indicates the amplifier reset watchdog has engaged. This is due to either a microprocessor fault condition or a cold start in progress. True indicates normal operation.

Bit 6 is false for normal operation. The bit is set true if factory check–out and tune–up is yet to be done (before shipment).

Bit 7 is the fault status indicator. False indicates that no faults exist. True indicates that a fault condition exists within the amplifier.

Address 01 Commands

Power on Command

The “power on” command causes the amplifier to perform its self initialization, self diag-nostics, and power–on sequence including tube warm–up delay. This sequence leaves the amplifier in the STANDBY mode with high voltage on to the tubes. Any mode and/or frequency information that may have been sent to the amplifier prior to this command is acted upon at the end of the initialization period. If a fault is detected during this sequence, an abort will occur and return the amplifier to the OFF mode.

NOTE:

If an amplifier restart (“power on” command) is attempted within fifteen sec-onds of being shut down from either the standby state or the operate state, the fast restart timing will result, and the six minute delay period is bypassed.

Section 3.2.1 SCM Commands (Continued)

Power off Command

The “power off” command causes the amplifier to execute its shutdown sequence of turning off tubes and opening relays ending in the OFF mode. The “power off” command also clears fatal and non–fatal faults (if the fault condition is no longer present).

Goto Operate Command

The “goto operate” command turns on the tube bias currents, enables the UNBLANK interrupt, enables AFT, and leaves the amplifier in the OPERATE mode.

Return to Ready Command

The “return to ready” command is the inverse of the “goto operate” command. This command is used to return the amplifier to the STANDBY mode. The “return to ready” command also clears non–fatal faults.

Address 02: “Change Mode” Byte

Write Bits:

Bits 0–3 are reserved for future use.

Bit 4 has no effect for writing.

Bits 5–6 are interpreted as a “change mode” command. Standard BCD weighting is used to define the mode number: 1 = Test; 2 = Head; 3 = Body.

Bit 7 is always written false.

Read Bits:

Bits 0–3 are reserved for future use.

Bit 4 always reads false.

Bits 5–6 echo the mode. Standard BCD weighting is used: 1 = Test; 2 = Head; 3 = Body.

Bit 7 always reads false.

Address 02 Commands

Change Mode command

The “change mode” is used to set the amplifier into one of the three modes of RF amplification and output. See Chapter 1, *Technical Specifications*, for mode output power levels and port assignments.

Section 3.2.1 SCM Commands (Continued)

If the amplifier is in the OPERATE state when the “change mode” command is received, a “mode command” fault 72 is generated (regardless of the new mode). Mode switching while in OPERATE could cause “hot switching” which could result in permanent damage or reduction of component life. The microprocessor protects against this occurrence by storing the “change mode” command and returning the amplifier to the STANDBY state. The fault condition is cleared when the “return to ready” command is received.

NOTE;

Even though the amplifier returns to STANDBY, a “return to ready” command has to be sent to clear the command fault.

If the amplifier is in the OFF state, the change is recognized and echoed, but will not occur until the “power on” command is received. If the amplifier is executing the “return to ready” command or is already in STANDBY, the command is executed immediately.

Address 03 “Change Frequency” Byte

Write Bits:

Bits 0–7 are the “frequency code”. A write to this address that changes any bits is interpreted as a “change frequency” command. Binary code 64 (40 hex) is used for 63.86 MHz operation.

NOTE;

In this amplifier, frequency codes other than 64 (40 hex) will result in a “frequency command fault” number 71.

Read Bits:

Bits 0–7 echo the “frequency code” stored at this address.

Address 03 Commands

Change Frequency command

The “change frequency”command is similar to the “change mode” command. If the amplifier is in the OFF state, the change is echoed and occurs when the “power on” command is received. The amplifier tunes itself to a factory preset configuration which matches the load at the selected frequency (only one frequency selection is allowed in this amplifier); the ‘Wait” status bit (address 01) is set true until the retuning process has been completed. If the amplifier is in OPERATE or a frequency code other than 40h is written, a frequency command fault 71 is generated, and the amplifier is returned to STANDBY.

Section 3.2.1 SCM Commands (Continued)

Address 04: “Fault Description” Byte

Read Bits (this is a read–only address):

Bits 07 echo the fault code associated with a fault condition within the amplifier. Fault codes are recorded in this latch within 10 milliseconds of detection. See Chapter 4 for a listing and description of all fault codes.

Table 3–1 SCM Addressing and Bit Assignment

ADDRESS	BIT	WRITE BITS	READ BITS
#01	0	power on/power off	power on/off command echo
	1	ret. to ready/goto operate	ready/operate command echo
	2	required to be false	wait status
	3	required to be false	amplifier in STANDBY
	4	required to be false	amplifier in OPERATE
	5	required to be false	microprocessor watchdog
	6	required to be false	factory tune–up indicator
	7	required to be false	fault status
#02	0	not used (no effect)	not used
	1	not used (no effect)	not used
	2	not used (no effect)	not used
	3	not used (no effect)	not used
	4	not used (no effect)	always false (for this amplifier)
	5	mode bit 0 (lsb)	mode bit 0 echo
	6	mode bit 1 (msb)	mode bit 1 echo
	7	required to be false	always false
#03	0	frequency bit 0	frequency bit 0 echo
	1	frequency bit 1	frequency bit 1 echo
	2	frequency bit 2	frequency bit 2 echo
	3	frequency bit 3	frequency bit 3 echo
	4	frequency bit 4	frequency bit 4 echo
	5	frequency bit 5	frequency bit 5 echo
	6	frequency bit 6	frequency bit 6 echo
	7	frequency bit 7	frequency bit 7 echo
#04	0	not used	fault code bit 0
	1	not used	fault code bit 1
	2	not used	fault code bit 2
	3	not used	fault code bit 3
	4	not used	fault code bit 4
	5	not used	fault code bit 5
	6	not used	fault code bit 6
	7	not used	fault code bit 7

Section 3.2.2 Serial Commands

In addition to the SCM commands, the amplifier can be controlled and diagnosed through an RS–232 interface located on the back of the amplifier (P2204 connector). This interface is intended to be supplemental to the SCM interface. However, it may be used in place of the SCM interface since all SCM commands and functions may be duplicated over the serial interface.

NOTE;

The SCM interface must be connected as described in Chapter 2, Section 2.2 and Chapter 3, Section 3.2.1 for the amplifier to operate. If incorrect connection is made to this interface (P2201 connector), a fault code 11 (see Chapter 4) will be displayed which will prohibit amplifier operation.

The SCM commands are sufficiently limited in that they cannot be used to operate the amplifier in an unsafe or nonstandard mode. The RS–232 commands, however, are quite general. In addition to the normal control functions available to the SCM interface, commands are available which can be used to defeat faults, open and close relays, and access the microprocessor's address space.

These "enhanced" commands allow much greater control of the amplifier and are very useful in identifying problems. However, they also allow some actions which will damage the amplifier if used indiscriminately; for example, it is possible to "hot switch" the relays, alter the power–up/down sequences, cause CW operation, etc. Consequently, extreme care should be used when controlling the amplifier over the serial interface.

RS–232 commands are formed from standard ASCII characters and are terminated with a carriage–return, (ASCII 0D hex). Upper and lower case letters can be used interchangeably. The "standard" commands have an SCM equivalent and can be used rather freely since they cannot result in abnormal operation. The "enhanced" commands enable the operator to configure the amplifier in a nonstandard way. These commands should be used with caution. Tables 3–2 and 3–3 summarize and describe all of the standard and enhanced serial commands respectively.

WARNING:

Enhanced commands should only be utilized as prescribed in officially documented procedures (several exist in Chapter 4). Permanent damage and hazardous conditions can be induced through improper use of these commands.

The implementation of RS–232 in this amplifier uses either 1200 or 9600 baud with no parity, 8 data bits, and 1 stop bit. The baud rate is determined by the contents of an EEPROM location (see Chapter 2, Section 2.2). The default baud rate is 9600.

3.2.2 Serial Commands (Continued)

Table 3.2 Standard Serial Commands

COMMAND	FUNCTION	DESCRIPTION
S	read status	Reads amplifier status; returns “busy” if wait flag is true or “ready, if wait flag is false.
o^0	power off	Return amplifier to OFF mode.
o^1	go to standby	Put or return amplifier to STANDBY mode.
o^3	go to operate	Put amplifier into OPERATE mode; valid only for amplifier in STANDBY mode (o1 command).
Test	TEST mode	Put amplifier in diagnostic TEST mode; 100 mW (maximum) RF output at J2504 connector.
Head	HEAD mode	Put amplifier in 2 KW HEAD mode of operation; RF output at J2803 connector.
Body	BODY mode	Put amplifier in 20 KW BODY mode of operation; RF output at J2804 connector.

Table 3.3 Enhanced Serial Commands

COMMAND	FUNCTION	DESCRIPTION
B+	disable synctab	Nine points called “synctab” are sampled outside of mainstream testing routine; B + disables the corresponding faults. Enter command only while the amplifier is in STANDBY mode.
B–	enable synctab	Opposite of B + command; synctab faults enabled Enter command only while in STANDBY mode.
B<n> n = 1–4	blast RF pulse	Generates 400 microsecond RF pulse from internal oscillator and sends it through amplifier to either RF Monitor dummy load resistor or output port. B1: HEAD mode – J2803 connector B2: HEAD mode – dummy load B3: BODY mode – J2804 connector B4: BODY mode – dummy load Synctab is updated for diagnostic purposes.
INIT	initialize amplifier	Used only at factory to initialize motor locations, RAM, type of UNBLANK circuity, DACs, and relays.

(Table 3–3 is continued on the next page.)

Section 3.2.2 Serial Commands (Continued)

Table 3.3 Enhanced Serial Commands (Continued)

COMMAND	FUNCTION	DESCRIPTION
MR<addr> addr = hex number	memory read	Reads an arbitrary address in microprocessors address space (do not enter brackets or a space between MR and address). Several addresses are output–only ports which are decoded in address space; any attempt to read these addresses will result in writing random data to it which can cause damage to amplifier.
MW<addr> <data> addr,data= hex number	memory write	Writes arbitrary data to an arbitrary address in the microprocessor's address space. This command requires a space delimiter between address and data (no space between command and address).
Z	zero motors	Drives the four motora to the zero stops while counting the steps. The required number of steps to reach zero is sent to the serial terminal. If the motor shafts are ever moved by hand, the motor zero positions will be lost. This command should then be used reinitialize the motors. Use only in OFF or STANDBY modes.
R <chan> chan=hex	read analog voltage	Reads arbitrary A/D channel (see Section 3.4.2, Table 2–14); can be used at any time
A<arg> arg = hex	set SS Latch	Sends "arg" byte Solid State Amplifier "SS Latch". One byte transfer is valid (00h–FFh) to set Solid State Amplifier switches and oscillator.
T<motor> <dest> motor= 1–4 dest = hex	turn motor	Turns motor to destination specified by "dest" number with respect to zero position. Turning motor past limit results in severe grinding sound; limit varies with each motor (see Table 2–1).
N <numb> numb = hex ASCII code	new tube	Copies new tube serial number and AFT motor positions into amplifier memory and zeros the tube "heater on–time" counter. If "numb" is just a car–riage return, only new motor positions are stored.
F	run subroutine	Executes the subroutine whose base address has been stored in the EEPROM "FCMD" location (see Section 3.4.2, Table 3–12).

Section 3.3 Microprocessor Utilization and Memory Allocation

The Erbtec MRI Amplifier is controlled and monitored by a Motorola MC68HC11 microcontroller (microprocessor). This microprocessor and all supportive circuitry are located on the Processor Board behind the AC Switching Module (see figures in Chapter 4, Service Manual. The Processor Board theory of operation may be found in the Section 2.2 of Chapter 2.

Section 3.3.1 Microprocsssor Overview

Overview

The microprocessor part numbers listed below are all suitable to control the MRI amplifier. Note, however, that they are not completely equivalent. The preferred microprocessor contains an evaluation ROM called “BUFFALO” which can be used for debugging purposes even if the external address bus becomes damaged or disfunctional. A complete description of BUFFALO including a source code listing can be obtained from Motorola technical manuals.

Table 3–4 Usable Microprocessor Part Numbers

MICROPROCESSOR	DESCRIPTION
XC6BHC11A8P1	Pre–production version; contains BUFFALO ROM
XC68HC11A1P	Pre–production version; no BUFFALO ROM
MC68HC11A8P1	Final production version; contains BUFFALO ROM
MC68HC11A1P	Final production version; no BUFFALO ROM

The 68HC11 contains a bit in an on–board (the microprocessor chip) EEPROM memory byte that enables/disables the BUFFALO ROM. If the device contains no ROM, this bit enables meaningless data bits. When the device is delivered from Motorola, the ROM (or meaningless data) is enabled.

This mode can be identified with an oscilloscope; there will be an E–clock but no address strobe because when BUFFALO is running, no external address is ever accessed. Consequently, most of the external support ICs such as the EPROM and the address latch are not utilized. This mode of operation can be useful for diagnosing a microprocessor problem.

Section 3.3.1 Microprocessor Overview (Continued)

Expanded Multiplexed Operating Modes

The 68HC11 is capable of several operating modes: expanded multiplexed, bootstrap, single chip, and test. The Erbtec MRI amplifier makes use of the expanded multiplexed and bootstrap modes. The different modes can be selected by jumpering the appropriate pins on MODA and MODB (see schematic set 86–013–2210 in the Service Manual, Chapter 5) and then forcing a reset. The normal operating mode as shipped from the factory is the “expanded multiplexed” mode. As such, there is an expansion bus with a full 64k memory map. The memory allocation is summarized in Section 3.3.2.

Summary of Chip Utilization

The 68HC11 has numerous on–board “controller” features which minimize the need for external circuitry to accomplish these tasks. This amplifier makes use of most of these features as described below (see also the Motorola MC68HC11A8/D Technical Data manual). Table 3–5 at the end of this Section details the complete pin–out of the microprocessor as used in the amplifier.

Pulse Accumulator is used as an external interrupt (independent enable) to flag a tube arc. The accumulator count is initialized to overflow minus one with interrupt on overflow enabled.

Timer Output compare TOC1 is used to measure the length of UNBLANK.

Timer Output compare TOC2 is used to interrupt the system for the purpose of testing the critical RF analog inputs (synctab).

Timer Output compare TOC3 controls the motor stepping and the motor acceleration ramp. Interrupts are used to drive the steps; hence, the stepping uncertainty equals the interrupt latency which is about 30 microseconds. This timer is never active while the pulse accumulator is enabled.

Timer Output Compare TOC4 is used as a general delay timer. This delay can not be used while any other timer interrupt is enabled. The delay routine is installed for future use only.

Timer Output Compare TOC5 is used to clock the Serial Peripheral interface (SPI). This interrupt is also never used while any other timer interrupt is enabled.

Serial Communications is RS–232 configured to operate at either 1200 or 9600 baud (determined by an EEPROM variable), no parity, 8 data bits, and 1 stop bit.
RDRF (receiver) Interrupt is enabled continuously. Bytes are collected in an input buffer (if space available) which is parsed and executed when a linefeed is received.
TDRE (transmitter) Interrupt is enabled only when a message is contained in the output buffer. When the last byte is transferred, the interrupt is disabled.

Section 3.3.1 Microprocessor Overview (Continued)

Serial Peripheral Interface (SPI) is used to drive the fault display and status LEDs on the Front Panel Display Board, and to control of the Solid State Amplifier Board (path switches, oscillator, and quad 6–bit "coarse" DAC for FET bias). This interface is not interrupt driven.

Table 3–5 Serial Peripheral Interface Usage

SIGNAL	BIT	FUNCTION
"ATTN"	bit 0	Attenuator switch control "A0"
	bit 1	Attenuator switch control "A1"
Solid State	bit 2	Attenuator switch control "A2"
Amplifier	bit 3	Attenuator switch control "A3"
	bit 4	J2503 RF IN connector enable "EXTRF"
	bit 5	Oscillator RF input enable "INTRF"
	bit 6	TEST mode J2504 connector enable "EXTOUT"
	bit 7	Oscillator on "OSM"
(these bits	bit 8–13	FET 1 coarse DAC
are optional)	bit 14–19	FET 2 coarse DAC
	bit 20–25	FET 3 coarse DAC
	bit 26–31	FET 4 coarse DAC
"STAT"	bit 0	OFF LED control
	bit 1	STANDBY LED control
Front Panel	bit 2	OPERATE LED control
Display	bit 3	WAIT LED control
	bit 4	HEAD MODE LED control
	bit 5	BODY MODE LED control
	bit 6	UNBLANK LED control
	bit 7	FAULT LED control
"CODE"	bits 0–3	FAULT CODE LED digit display, right–side digit
Fr. Pan. Dis.	bits 4–7	FAULT CODE left–side digit

On–board A/D converters are enabled and configured in the continuous scan mode; these four channels cannot be interrupt driven. Converted data represents the voltage at the analog test point at some point within the last 64 microseconds; cycle time is every 64 microseconds.

EEPROM programmable read–only memory allocation and function is listed in Section 3.4.2, Table 3–12.

COP "Watchdog" system is programmed to fire at 262.144ms if the firmware does not reset the timer. The dog is reset in the main firmware operating loop and during one of the timer interrupt routines.

Section 3.3.1 Microprocessor Overview (Continued)

RTC real time clock is interrupt driven and is used by the delay and the tube “heater on–time” routines. In addition, the interrupt handler checks the RS–232 CTS line. This timer ticks every 16.384ms.

HPRIO is used to force the pulse accumulator overflow interrupt (tube arc) to the highest priority. This means that the interrupt latency for a tube arc is equal to the interrupt latency of the system; latency is approximately 30us.

Table 3–6 Summary of 68HC11 Pin Allocation

PIN #	SIGNAL NAME	DESCRIPTION
25 24	MODA MODB	Used to set operating mode. Normal mode is the “Expanded Multiplexed”; jumperable to “Single–Chip” or Bootstrap”. In the Single chip mode, the Buffalo monitor will run if appropriate version of the HC11 is installed as described in Table 34.
	PORTA:	General input/output
8	PA0	Safety interlock input “RF INTLK”
7	PA1	Safety relay sense input
6	PA2	Serial “CTS” input
5	PA3	Fault indicator interlock output “FLT INTLK”
4	PA4	Internal RF gating output “INTERNAL RF ON”
3	PA5	UNBLANK interrupt enable output
2	PA6	UNBLANK interrupt enable output
1	PA7	Tube arc interrupt output
	PORT B:	High–order half of external expansion address bus
16	PB0	Address bus bit 8
15	PB1	Address bus bit 9
14	PB2	Address bus bit 10
13	PB3	Address bus bit 11
12	PB4	Address bus bit 12
11	PB5	Address bus bit 13
10	PB6	Address bus bit 14
9	PB7	Address bus bit 15
	PORTC:	Low–order half of address bus (shared as data I/O)
31	PC0	Address/Data bus bit 0
32	PC1	Address/Data bus bit 1
33	PC2	Address/Data bus bit 2
34	PC3	Address/Data bus bit 3
35	PC4	Address/Data bus bit 4
36	PC5	Address/Data bus bit 5
37	PC6	Address/Data bus bit 6
38	PC7	Address/Data bus bit 7

(Table 3–6 is continued on the next two pages.)

Section 3.3.1 Microprocessor Overview (Continued)

Table 3–6 68HC11 Pin Allocation (Continued)

PIN #	SIGNAL NAME	DESCRIPTION
	PORTD:	Serial communication interfaces (SCI and SPI)
42	PD0	SCI receive data line “RxD”
43	PD1	SCI transmit data line “TxD”
44	PD2	SPI master in, slave out line “MISO” (not used)
45	PD3	SPI master out, slave in line “MOSI”
46	PD4	SPI serial clock “SCK”
47	PD5	SPI slave select “/SS”
	PORTE:	Multiplexed A/D channels
17	PE0	Channel 1 A/D converter
	“IPA FOR PWR”	HEAD mode forward power
	“IPA GRID I MON”	IPA tube grid current
	“IPA V BIAS MON”	IPA tube cathode to grid voltage
	“FAN AIR 1 ”	Fan pressure transducer ambient reference
	“IPA PLATE 1”	IPA tube plate current
	“HS MON”	Thermistor on Solid State Amplifier
	” + UNREG”	Line voltage monitor
	“PA TUNE”	PA Phase Detector
18	PE1	Channel 2 A/D converter
	“PA FOR PWR”	BODY mode forward power
	“PA GRID I MON”	PA tube grid current
	“PA V BIAS MON”	PA tube cathode to grid voltage
	“FAN AIR 2”	Fan pressure transducer flow sensor
	“PA PLATE 1”	PA tube plate current
	“SCM CAB. MON”	SCM cable present check
	“IPA TUNE”	IPA phase detector
	” + 100V MON”	+ 100 volt supply
19	PE2	Channel 3 A/D converter
	“IPA REF PWR”	HEAD mode reflected power
	“IPA HV”	+3KV supply
	“IPA HTR I MON”	IPA tube heater current
	“IPA ANODE RF”	IPA envelope detector
	“–5V MON”	–5 volt supply
	“MOTOR DRIVE 1”	Motor 1 and motor 2 driver
	“SS AMP I MON”	Solid State Amplifier FET bias currents
	” +48V MON”	+48 volt supply
20	PE3	Channel 4 A/D converter
	“PA REF PWR”	BODY mode reflected power
	“PA HV”	+6n supply
	“PA HTR I MON”	PA tube heater current
	“TUBE AIR 2”	VTAC pressure transducer
	” +32V MON”	+32 volt supply
	“MOTOR DRIVE 2”	Motor 3 and motor 4 driver
	” +2.5V REF”	+5 volt supply
	“+24V MON”	+24 volt supply

Section 3.3.1 Microprocessor Overview (Continued)

Table 3–6 68HC11 Pin Allocation (Continued)

PIN #	SIGNAL NAME	DESCRIPTION
	Miscellaneous:	Chip support pins
21	VRL	A/D reference low voltage, ground
22	VRH	A/D reference high voltage, +5 volts
23	V3S	Ground
26	AS	Address strobe
27	E	System “E–clock” output
28	RM	Read and write enable
29	EXTAL	8.0 MHZ clock input
30	XTAL	Crystal driver
39	RESET	Microprocessor forced reset
40	XIRO	External interrupts (unused)
41	IRO	Interrupt request input for UNBLANK
48	VDD	+5 volts

Section 3.3.2 Memory Allocation Summary

Table 3–7 provides a block summary of the memory and addressing used in the amplifier. Details of memory allocation appear in the tables to follow.

Table 3.7 Address Map Summary

ADDRESS	DESCRIPTION
0000–00FF	RAM on–board 68HC11 microprocessor
0100–0FFF	Unused
1000–103F	Internal 68HC1 1 microprocessor registers
1040–1FFF	Unused
2000–2FFF	Decoded output ports
3000–3FFF	Dual port RAM chip
4000–4FFF	Motor 1 and motor 2 drive latch
5000–5FFF	Motor 3 and motor 4 drive latch
6000–5FFF	Relay drive latch
7000–7FFF	General input data
8000–B5F F	EPROM (if 27256 chip used)
B600–B7FF	EPROM on–board 68HC11 microprocessor
C000–DFFF	EPROM (if 27122 chip used)
E000–FFFF	EPROM (if 2764 chip used)

Section 3.3.2 Memory Allocation Summary (Continued)

On–board RAM Allocation Summary

The 68HC11 comes with 256 bytes of on–board RAM. Specific address assignments are made by a relocatable linker that changes these addresses with each firmware revision. Table 3–8 shows the few RAM addresses and associated variables that are independent of the linker.

Table 3–8 Fixed RAM Variables

ADDR	BIT	DESCRIPTION
0000		SYSFLAG
	bit 0	selfest OK
	bit 1	fan fault enable
	bit 2	background refresh enable
	bit 3	microprocessor shutdown occurring
	bit 4	run disable
	bit 5	system initialization complete
	bit 6	28V supply stable
	bit 7	task 2 enabled
0001		CMDFLG
	bit 0	exit
	bit 1	fault
	bit 2	fast restart
	bit 3	aft completed
	bit 4	non–fatal fault
	bit 5	service mode
	bit 6	SCM state variable
	bit 7	serial message enable
0002		DEBUGFLAG
	bit 0	AFT disable
	bit 1	Motor initialize
	bit 2	UNBLANK enable
	bits 3–7	Undefined
0003–00DF		Miscellaneous RAM variables
00E0		Lowest Point on Stack (approximate)
00FF		Top of Stack

Section 3.3.2 Memory Allocation Summary (Continued)

External Address Map Summary

Table 3–9 summarizes the entire “expanded multiplexed” mode “external” addressing scheme. These addresses are called external since they do not exist within the 68HC11 on–board RAM (0000–00FF) or EEPROM (B600–B7FF). This table describes each of the memory blocks of Table 3–7 in more detail.

Table 3–9 External Address Summary

ADDRESS	DESCRIPTION
2000–2FFF	Decoding of “CS2” (see schematics) signal lines:
2000	“FET1” fine bias DAC latch enable
2001	“FET2” fine bias DAC latch enable
2002	“FET3” fine bias DAC latch enable
2003	“FET4” fine bias DAC latch enable
2004	“TUBE1” (IPA) cathode bias DAC latch enable
2005	“TUBE2” (PA) cathode bias DAC latch enable
2006	Latch enable for “ENA1”–”ENA4” and “/(I)PA GATE” enable bits
2007	Latch enable for A/D mux control bits “A”, “B”, “C”; SPI control bits “ATTN”, “STAT”, “CODE”; RS–232 “DTR”; “/EXT RF ON” gate
3000–3FFF	Dual Port RAM
3000	SCM write 00 address (unused)
3001	SCM write 01 address (commands): bit 0 = power on/off bit 1 = ready/operate bit 2–7 = must be false
3002	SCM write 02 address (mode): bit 0–7 =20h = TEST mode =40h = HEAD mode =60h = BODY mode
3003	SCM write 03 address (frequency): bit 0–7 = 40h (only valid value)
3004	SCM write 04 address (not allowed)
3005–300F	SCM write 0x address (supplemental) where x = 5, 6, 7
3010	SCM read 00 address (unused)
3011	SCM read 01 address (command echo): bit 0 = power on/off command bit 1 = ready/operate command bit 2 = wait status bit 3 = STANDBY mode bit 4 = OPERATE mode bit 5 = watchdog status bit 6 = factory tune complete bit 7 = fault status
3012	SCM read 02 address (mode echo): bit 0–3 = not used bit 4, 7 = false bit 5–6 = mode

Section 3.3.2 Memory Allocation Summary (Continued)

Table 3–9 External Address Summary (Continued)

ADDRESS	DESCRIPTION
3013	SCM read 03 address (frequency echo) bit 0–7 = 40h only
3014	SCM read 04 address = fault code
3015–301F	SCM read 0x address (supplemental) where x =5, 6, 7...
3020–00FF	Miscellaneous RAM variables
3100–3107	Semaphore read registers
3110–3117	Semaphore write registers
4000–4FFF	Motor Driver 1 control where “A” = Motor 1, “B” = Motor 2
5000–5FFF	Motor Driver 2 control where “C” = Motor 3, “D” = Motor 4
6000–6FFF	Relay and tube heater control: “HEATER ENABLE” = IPA and PA tube heaters “RF RLY1–3” = relays in VTAC (1), RF Monitor (2=K1, 3=K2) “100V RUN, START RLY” = Low Volt. Trans. run and soft–start “HV RUN, START RLY” = 4.5nA HV Trans. run and soft–start
7000–7FFF	Miscellaneous digital inputs: “COVER SW1,2” = cover safety switches “ZSENSE 1–4” = motor zero sensora “CARRIER” = RS–232 carrier detect
8000–FFFF	EPROM
8000	Starting address if 27256 chip used
C000	Starting address if 27128 chip used
E000	Starting address if 2764 chip used

Section 3.4 Reading Microprocessor Data

It is possible to obtain the data stored in the microprocessor memory by following the procedures outlined in this Chapter. The SCM interface can be used only to read data; whereas, the RS–232 interface allows for both reading and writing of address space.

WARNING:

Writing (and even some reading) of data over the serial interface can be hazardous to personnel and can cause permanent damage to the amplifier. Follow officially documented procedures only for data access using the RS–232 interface.

Both SCM and RS–232 procedures for reading data are outlined. Microprocessor data is encoded for easy access over the SCM interface, and this encoding also avoids complications of following absolute address variations with linkers and firmware revisions. A serial method of replicating the SCM data access protocol is presented for use of these codes with the RS–232 interface.

Section 3.4.1 Data Access Method

SCM Method

As described in Section 3.2, the SCM interface uses the four “addresses” 01–04 to control and monitor the Erbtec MRI Amplifier. Supplemental SCM addresses 05 and 06 have also been provided so that microprocessor data not ordinarily required for normal operation can be read for diagnostic purposes.

1. Look up the desired Memory Access Code (Section 3.4.2, Table 3–10) and Data Code (Section 3.4.2, Tables 3–11 through 3–14).
2. Write the desired Address Code to SCM address 06.
3. Write the desired Memory Access Code to SCM address 05.
4. Read data continually from address 05 until the value 255 (0FFh) is read. This is part of the handshaking process.
5. Read the microprocessor data associated with the Address Code from dress 06.
6. Write “00” to address 05.
7. Read data from address 05 until value 0 is read completing the handshake.

Serial RS–232 method

The SCM method described above may be safely duplicated on the serial interface by using the enhanced commands “MW” and “MR” with the procedure described here. Any of the Address Codes in Tables 3–11 through 3–14 may be read in this manner.

1. Look up the desired Memory Access Code (Section 3.4.2, Table 3–10) and Data Code (Section 3.4.2, Tables 3–11 through 3–14).
2. Use the “MU” command to write the desired Address Code to absolute memory address 3006h.
3. Use the “MW” command to write the Memory Access Code to address 3005h.
4. Use the “MR” command to read absolute memory address 3015h until value 255 (0FFh) is read to initiate the handshaking process.
5. Use the “MR” command to read the microprocessor data associated with the Address Code from memory address 3016h.
6. Use the “MW” command to write “00” to absolute memory address 3005h.
7. Use the “MR” command to read data continually from absolute memory dress 3015h until the value 0 is read completing the handshake.

Section 3.4.2 Data Access Codes

The firmware source code for the microprocessor is contained in several (more than twelve) separate assembly language files. Each of these files declares certain RAM variables that are assembled into the machine code without reference to absolute addresses. During the final linking, absolute addresses are assigned by the linker.

The absolute address of these variables changes from one revision of the firmware to another. However, the variable name itself, does not change. So rather than referencing these variables by their absolute address, an encoded table was created in one of the source files that correlates the variable name with an access code that is independent of the linking process.

The tables in this Section provide a complete listing of the Address Codes and the corresponding firmware variable name or assignment. For most variables, a brief description of the function is also included.

Access to the variable value located by an Address Code must first begin with a specification as to where in memory to apply the Address Code. Microprocessor memory access has been subdivided into four sections: RAM (Table 3–11), EEPROM (Table 3–12), 68HC11 Registers (Table 3–13), and A/D Conversions (Table 3–14).

Each of these four memory subdivisions has an Address Code 00, 01, etc. Therefore, a Memory Access Code (Table 3–10 below) is used to first indicate which memory division to access. See the procedures detailed in Section 3.4.1 for the complete discussion of how to use these codes.

NOTE:

All access codes and absolute addresses mentioned in this Chapter are in hexadecimal notation unless otherwise noted.

Table 3–10 Memory Access Codes

CODE	MEMORY DIVISION ACCESSED
FC	Global RAM variables
FD	EEPROM addresses
FE	68HC11 internal registers
FF	Make A/D conversion and transfer result

Section 3.4.2 Data Access Codes (Continued)

Table 3–11 RAM Address Codes

NOTE:

The absolute memory address associated with each RAM Address Code may be found through procedure described in Section 2.2, Chapter 2.

CODE	VARIABLE	DESCRIPTION
00	FET1,2 Bias Current Target	Bias current for each MRF148 FET on Solid State Amplifier; set and sustained by microprocessor.
01	FET3,4 Bias Current Target	Bias current for each MRF150 FET on Solid State Amplifier; set and sustained by microprocessor.
02	Tube1 (IPA) Bias Current Target	Bias current for 3CPX800A7tube; set (not sustained) by the microprocessor for each mode
03	Tube2 (PA) Bias Current Target	Bias current for YC156 tube; set (not sustained) by the microprocessor for BODY mode
04 05 06 07	FET 1, 2, 3, 4 Coarse DACs	DACs used to control MRF148 and MRF150 FET gate voltages to set “ballpark” bias currents
08 09 0A 0B	FET1, 2, 3, 4 Fine DACs	DACs used to control MRF148 and MRF150 FET gate voltages to accurately set and maintain bias current
0C	Tube1 DAC	DAC used as part of 3CPX800A7 grid bias control
0D	Tube2 DAC	DAC used as part of YC–156 grid bias control
0E	Nominal Attenuator	Value written to Solid State Amplifier step attenuator when an UNBLANK is received; mode dependent
0F	Attenuator Copy	Current contents S.S. Amp. step attenuator latch
10 11	Motor1 (msb) (lsb)	Current motor 1 position
12 13	Motor2 (msb) (lsb)	Current motor 2 position
14 15	Motor3 (msb) (lsb)	Current motor 2 position
16 17	Motor 4 (msb) (lsb)	Current motor 4 position
18	Relay Port Copy	Copy of relay control output–only port for reading
19 1A	2006 Port Copy 2007 Port Copy	Copy of absolute addresses 2006h and 2007h which are output–only miscellaneous enable bits

Table 3–11 is continued on the next page.)

Section 3.4.2 Data Access Codes (Continued)

Table 3–11 RAM Address Codes (Continued)

CODE	DATA	DESCRIPTION
1B	Operate State	Current amplifier operate mode; 00 = OFF, 01 = STANDBY, 03 = OPERATE
1C	SYSFLAG	System status bits: bit 0 = selftest OK, bit 1 = fan fault enable, bit 2 = background refresh enable, bit 3 = main power failure, bit 4 = run disable, bit 5 = system initialization complete, bit 6 = +28V supply stable, bit 7 = task 2 enabled
1D	CMDFLAG	System control bits: bit 0 = exit, bit 1 = fault, bit 2 = fast restart, bit 3 = aft completed, bit 4 = non–fatal fault, bit 5 = service mode, bit 6 = SCM state variable, bit 7 = serial message enable
1E	FCODE	Number currently displayed on the Front Panel Display; 0AAh results in a blank display
1F	SCODE	Byte mapped onto the eight status LEDs on the Front Pan. Disp.; bit 0 = OFF..... bit 7 = FAULT
20 21 22 23	System Time 0 System Time 1 System Time 2 System Time 3	Main clock in the amplifier initialized at the completion of the selfest; counts elapsed time in units of 16.384 milliseconds
24 25 26 27 28 29 2A 2B	Inptr+0 Inptr+1 Outptr+0 Outptr+1 Prsptr+0 Prsptr+1 Outmax+0 Outmax+1	RS–232 buffer pointers
2C	PHTARG	“Zero” level phase detect value during BLANK
2D	PHREAL	Last actual reading taken from either phase detector

(Table 3–11 is continued on the next page.)

Section 3.4.2 Data Access Codes (Continued)

Table 3–11 RAM Address Codes (Continued)

CODE	DATA	DESCRIPTION
2E	Max	Miscellaneous AFT variables used by the firmware
2F	Target	to execute PA tube AFT
30	FP	
31	Pos1 +0	
32	Pos1 +1	
33	Pos2+0	
34	Pos2+1	
35	HV Target	
36	Timecopy +0	Copy of least significant 2 bytes of System time;
37	Timecopy + 1	used for OFF to STANDBY delay timing by firmware
38	HTIME +0	Current–mode tube heater on–time counters; time to
39	HTIME +1	be added to TTLHEAT and tube on–time counters
3A	HTIME +2	at next OFF mode
3B	HTIME +3	
3C	Run 2006	Contents of output–only control port address 2006h for use at UNBLANK interrupt
3D	REF Flags	Collection of flags used by firmware to enable or disable selected faults
3E	AREG Save	Byte containing contents of microprocessor accumu–lator when a fault is detected; last analog conversion data stored here if fault is due to A/D out of range.
3F	SYNCTAB +0	PA forward power latest A/D conversion
40	SYNCTAB +1	IPA forward power
41	SYNCTAB +2	PA plate current
42	SYNCTAB +3	IPA plate current
43	SYNCTAB +4	PA grid current
44	SYNCTAB +5	IPA grid current
45	SYNCTAB +6	PA refiected power
46	SYNCTAB +7	IPA reflected power
47	SYNCTAB +8	IPA envelope
48		reserved for future use
49	IPA Phase	A/D of IPA phase detector at last UNBLANK
4A	PA phase	A/D of PA phase detector at last UNBLANK
4B	IPA Envelop	A/D of IPA envelope transducer at last UNBLANK
4C	SCM Table (msb)	Data used to locate absolute address of RAM
4D	SCM Table (Isb)	Address Codes; differs with each firmware rev.
4E	Time Left +0	Time remaining in 6 minute OFF to STANDBY
4F	Time Left +1	warm–up period

(Table 3–11 is continued on the next page.)

Section 3.4.2 Data Access Codes (Continued)

Table 3–11 RAM Address Codes (Continued)

CODE	DATA	DESCRIPTION
50	Motor Fault +0	Microprocessor calculated position of motor at last
51	Motor Fault +1	motor fault
52	AFT Power	A/D of IPA envelope during last AFT

Table 3–12 EEPROM Address Codes

NOTE:

The absolute memory address associated with each EEPROM Address Code is B600h + code; for example, PATARG is memory address B623h.

CODE	DATA	DESCRIPTION
00	PANBASE	Index to base address of “Panic Block”; power failures
01	TPARMS	Index to base address of “Tuning Block”; motor tune
02	MAINT	Index to base address of “Maintenance Block”
03	REVNUM (msb)	Revision number of firmware
04	REVNUM (msb)	
05	SERNUM (msb)	Amplifier serial number (with Processor Board)
06	SHIP (msb)	Date amplifier or Processor Board shipped
07	SHIP (lsb)	
08	SERVICE (msb)	Last date amplifier or Processor Board serviced
09	SERVICE(lsb)	at Erbtec
10	PCOUNT (msb)	Panic Block EEPROM write–ctcle counter; used
11	PCOUNT (lsb)	during power failure
12	TTLHEAT (msb)	Total tube heater on–time of amplifier since shipment
13	TTLHEAT	
14	TTLHEAT	
15	TTLHEAT (lsb)	
16	LAST FLT	Fault code of last fatal fault during OPERATE mode
20	FANDIFF	Used for fan fauit detection
21	FANENA	Fan fault enable; 00 = enable, else disable
22	IPATARG(BODY)	BODY mode IPA tube bias current target
23	PATARG	PA tube bias current target
24	RS–232 CONFIG	Configuration of RS–232 parameters

(Table 3–12 is continued on the next page.)

Section 3.4.2 Data Access Codes (Continued)

Table 3–12 EEPROM Address Codes (Continued)

CODE	DATA	DESCRIPTION
25	PA AFTENA	Enable of PA tube AFT; 00 = enable, else disable
26	FAN NUM	Number of fans in amplifier; FF= 1 fan, 02=2 fans
27	IPATARG(HEAD)	HEAD mode IPA tube bias current target
28	ATTNCFG	Gain correction factor of Solid State Amp. (not used)
29	FCMD (msb)	index to base address of subroutine to be executed
2A	FCMD (lsb)	by the serial “F” command
2B	AFTENA	Enable amplifier AFT; 00 = enable, FF = disable
2C	TUNEENV	IPA envelope value at 1KW of power
2D	PACORR (msb)	Motor 3 offset used to precisely center bandwidth
2E	PACORR (lsb)	after AFT
30	PANSPARE	Spare “Panic Block” (for future use)
50	MOT1A (msb)	HEAD mode “Tune Block” motor positions after
51	MOT1A (lsb)	AFT occura
52	MOT2A (msb)	
53	MOT2A (lsb)	
54	MOT3A (msb)	
55	MOT3A (lsb)	
56	MOT4A (msb)	
57	MOT4A (lsb)	
58	MOT1 B (msb)	BODY mode “Tune Block” motor positions after
59	MOT1 B (lsb)	AFT occurs
5A	MOT2B (msb)	
5B	MOT2B (lsb)	
5C	MOT3B (msb)	
5D	MOT3B (lsb)	
5E	MOT4B (msb)	
5F	MOT4B (lsb)	
60	MOT1C (msb)	HEAD mode “Tune Block” motor positions as set
61	MOT1C (lsb)	at factory
62	MOT2C (msb)	
63	MOT2C (lsb)	
64	MOT3C (msb)	
65	MOT3C (lsb)	
66	MOT4C (msb)	
67	MOT4C (lsb)	

(Table 3–12 is continued on the next page.)

Section 3.4.2 Data Access Codes (Continued)

Table 3–12 EEPROM Address Codes (Continued)

CODE	DATA	DESCRIPTION
68	MOT1D (msb)	BODY mode “Tune Block” motor positions as set
69	MOT1D (lsb)	at factory
6A	MOT2D (msb)	
6B	MOT2D (lsb)	
6C	MOT3D (msb)	
6D	MOT3D (lsb)	
6E	MOT4D (msb)	
6F	MOT4D (lsb)	
70–77	IPA SERNUM	IPA tube serial number (70= msb, 77=lsb)
78–7B	IPA HEAT	IPA tube heater on–time counter (78= msb, 7B =isb)
80–87	PA SERNUM	PA tube serial number (80=msb, 87=lsb)
88–8B	PA HEAT	PA tube heater on–time counter (88= msb, 8B =lsb)

Table 3–13 68HC11 Register Address Codes

NOTE:

The absolute memory address associated with each 68HC11 Register Address Code is 1000h + code; for example, BAUD is at address 102Bh. See the Motorola MC68HC1 1A8 technical reference manual for register descriptions.

CODE	DATA
00	PORTA
01	reserved by Motorola
02	PIOC
03	PORTC
04	PORTB
05	PORTCL
06	reserved by Motorola
07	PIOC
08	PORTD
09	DDRD
0A	PORTE

(Table 3–13 is continued on the next page.)

Section 3.4.2 Data Access Codes (Continued)

Table 3–13 68HCJ1 Register Address Codes (Continued)

CODE	DATA
0B	CFORC
0C	OC1M
0D	OC1D
0E	TCNT
10	TIC1 (msb)
11	T1C1 (lsb)
12	TIC2 (msb)
13	TIC2 (lsb)
14	TIC3 (msb)
15	TIC3 (lsb)
16	TOC1 (msb)
17	TOC1 (lsb)
18	TOC2 (msb)
19	TOC2 (lsb)
1A	TOC3 (msb)
1B	TOC3 (lsb)
1C	TOC4 (msb)
1D	TOC4 (lsb)
1E	TOC5 (msb)
1F	TOC5 (lsb)
20	TCTL1
21	TCTL2
22	TMSK1
23	TFLG1
24	TMSK2
25	TFLG2
26	PACTL
27	PACNT
28	SPCR
29	SPSR
2A	SCDR

(Table 3–13 is continued on the next page.)

Section 3.4.2 Data Access Codes (Continued)

Table 3–13 68HC11 Register Address Codes (Continued)

CODE	DATA
2B	BAUD
2C	SCCR1
2D	SCCR2
2E	SCSR
2F	SCDR
30	ADCTL
31	ADR1
32	ADR2
33	ADR3
34	ADR4
35	reserved by Motorola
36	reserved by Motorola
37	reserved by Motorola
38	reserved by Motorola
39	OPTION
3A	COPRST
3B	PPROG
3C	HPRIO
3D	INIT
3E	TEST1
3F	CONFIG

Section 3.4.2 Data Access Codes (Continued)

Table 3–14 A/D Address Codes

NOTE:

There is no actual absolute memory address associated with these codes. Accessing an A/D Address Code causes the microprocessor to make the named A/D conversion and transfer the result for output.

CODE	DATA	DESCRIPTION
00	IPA FOR PWR	HEAD mode forward power output
01	IPA GRID I MON	IPA tube grid current
02	IPA V BIAS MON	PA tube cathode to grid bias voltage
03	FAN AIR 1	Fan pressure transducer ambient reference
04	IPA PLATE I	IPA tube plate current
05	HS MON	Thermistor on Soiid State Amplifier
06	+ UNREG	Line voltage monitor
07	PA TUNE	PA Phase Detector output
08	PA FOR PWR	BODY mode forward power output
09	PA GRID I MON	PA tube grid current
0A	PA V BIAS MON	PA tube cathode to grid bias voltage
0B	FAN AIR 2	Fan pressure transducer in HV Cavity (bottom)
0C	PA PLATE I	PA tube plate current
0D	SCM CAB. MON	SCM cable presence check
0E	IPA TUNE	IPA phase detector
0F	+100V MON	+ 100volt supply
10	IPA REF PWR	HEAD mode refiected power
11	IPA HV	+3KV supply
12	IPA HTR I MON	IPA tube heater current
13	IPA ANODE RF	IPA envelope detector
14	–5V MON	–5 volt supply
15	MOTOR DRIVE 1	Motor 1 and motor 2 driver
16	SS AMP I MON	Solid State Amplifier FET current
17	+48V MON	+48 volt supply
18	PA REF PWR	BODY mode reflected power
19	PA HV	+6KV supply
1A	PA HTR I MON	PA tube heater current
1B	TUBE AIR 2	VTAC pressure transducer
1C	+32V MON	+32 volt supply
1D	MOTOR DRIVE 2	Motor 3 and motor 4 driver
1E	+2.5V REF	+5 volt supply through 2.5 volt reference
1F	+24V MON	+24volt supply

Section 3.5 Microprocessor Functional Chronologies

This Section describes the general algorithms used by the amplifier's microprocessor to perform normal operations such as changing modes and executing commands. This information can be very useful for diagnostic purposes.

OFF to STANDBY

1. Store mode (HEAD or BODY).
2. Disable RF paths and UNBLANK.
3. Max the Solid State Amplifier step attenuator.
4. Initialize power supply and RF relays.
5. Initialize arc detection.
6. If arc–detect circuit failure, fault code 87.
7. Start +100 volt supply.
8. Pause 1.00 second
9. If + 100 volt supply less than 85 volts, fault code 50.
10. Run + 100V supply.
11. Wait 100 milliseconds.
12. If + 100 volt supply less than 90 volts, fault code 51
13. Enable tube heaters.
14. Record system time to calculate accumulative heater on–time.
15. Wait 1.00 second.
16. If IPA heater current out of range, fault code 52.
17. If PA heater current out of range, fault code 53.
18. Wait 15 seconds.
19. Enable fan and blower faults; check every 1.5 milliseconds.
20. Set Motor positions.
21. Wait for the balance of 360 second time–out.
22. Enable fast restart.
23. Start high voltage supplies.
24. Track HV supplies for 5 seconds.
25. If HV supplies out of range, fault code 57 or 58 (+3K or +6KV).
26. Run high voltage supplies.
27. Wait 100 milliseconds.
28. Initialize tube bias DACs.
29. Test high voltage supplies.
30. Wait 1.0 second.
31. Initialize FET bias currents ("ballpark").
32. Enable all high voltage faults.
33. Set RF relays to "safe" positions for maximum RF isolation from outside world.

Section 3.5 Microprocessor Functional Chronologies (Continued)

STANDBY to OPERATE

1. Disable FET background refresh.
2. Disable RF paths and UNBLANK
3. Max Solid State Amplifier step attenuator.
4. If TEST mode, disable both tubes.
5. Configure step attenuator for chosen mode.
6. If non–service mode, enable tlmer interrupt.
7. Set IPA tube and PA tube bias currents for selected mode.
8. Update FET bias currents.
9. Execute AFT.
10. Set RF relays for selected mode.
11. Initiaiize and enable UNBLANK interrupt.

OPERATE to STANDBY

1. Disable high voltage interrupt tlmer.
2. Disable UNBLANK.
3. Disable tube bias circuits.
4. Wait 100 milliseconds.
5. Set RF relays to “safe” positions for maximum isolation from external world.
6. Enable FET coarse bias refresh.

STANDBY to OFF

1. Disable fan and blower faults.
2. Disable FET background refresh.
3. Disable high voltage faults.
4. If high voltage run is engaged, drop HV run relay.
5. Wait 100 milliseconds.
6. Disable arc detect circuitry.
7. If high voltage start relay engaged, drop HV start relay.
8. Wait 100 milliseconds.
9. Enable internal RF gate to bleed HV capacitors.
10. Decrease tube DACs to 0.00 volts.
11. Wait 15.1 seconds.
12. Re–initialize tube dacs.
13. Disable internal RF gate.
14. Disable IPA and PA bias gates.
15. Disable fast restart flag.
16. Disable tube heater power.
17. UNBLANK FET stages.
18. Wait 5.00 seconds.
19. BLANK FET stages.
20. Drop 100 volt run relay.
21. Wait 100 milliseconds.
22. Drop 100v start relay

Section 3.5 Microprocessor Functional Chronologies (Contined)

Pulse Accumulator Interrupt (Tube Arc)

1. Disable external UNBLANK.
2. Drop high voltage run relay.
3. If PA plate current A/D value greater than 250, fault code 86, else fault code 81.
4. Wait 10 milliseconds.
5. Drop high voltage start relay.
6. Wait 15 milliseconds.
7. Disable the “Tube Arc” interrupt.
8. Resume normal power–off sequence.

UNBLANK interrupt

1. Disable internal RF oscillator.
2. Enable all FETs on Solid State Amplifier.
3. Set Solid State Amplifier step attenuator to nominal value.
4. Extemal RF gates on.
5. Enable BLANK interrupt.
6. Configure UNBLANK timer to interrupt in 20.00 milliseconds.

BLANK interrupt

1. Enable UNBLANK interrupt.
2. Disable all FETs on Solid State Amplifier.
3. Disable 20 millisecond UNBLANK timer.
4. Set Solid State Amplifier step attenuator to maximum attenuation.

Background Tests

The microprocessor also operates in a loop that tests the hardware for normal operational conditions. These tests are performed continuously, whenever the circuit breaker CB1 on rear panel is on. If any background test fails, a fault code is displayed on the two front panel 7–segment displays. Power is automatically disabled, and the amplifier is returned to a safe operating state. Usually, a safe operating state means discharging the power supplies and returning the amplifier to the OFF mode as quickly as possible. Fault conditions that cause this response are called “fatal.” Other faults are called “non–fatal” and result in disabling UNBLANK and returning the amplifier to STANDBY.

1. Check external safety: cover interlock 1 (fault 82), cover interiock 2 (fault 83), 12V external relay power loss (fault 85), external “RF MON” cable connected (fault 84).
2. Check + UNREG supply for low line voltage (fault 92).
3. Check blower and fan sensors to ensure proper air flow.
4. Check all power supply voltages for tolerance values.
5. Check SCM interlock for proper connection to external control computer.
6. Check tube heaters for current within tolerance.
7. Check Solid State Amplifier thermistor for excessive temperature.

CHAPTER 4 DIAGNOSTICS

Section 4.1 Equipment Safety Considerations

The Erbtec 86–013–0000 MRI Amplifier has been designed with considerable attention to safety. Numerous internal points are monitored by the microprocessor to check for irregularities in amplifier operation. For the safety of the patients, operator, and for the safety of the amplifier itself, any internal (and a few external) irregularities detected by the amplifier's microprocessor will cause the amplifier to completely or partially shutdown and issue an associated fault code. Fault code definitions are found in Section 4.2 of this Chapter.

The amplifier has built–in safety "cover interlock" switches that fault the amplifier when a cover panel is removed. This keeps the amplifier in an OFF mode when the covers are removed. If a power–on mode should be required for servicing or diagnostics, these safety switches may be overridden. This level of servicing is generally discouraged and is not ordinarily required. Most diagnostics may be done by first reading significant microprocessor memory locations (see Chapter 3), and then confirming the diagnosis by making measurements on the troubled module while in an OFF condition.

WARNING:

Extreme is required when overriding the cover safety switches. There are lethal voltages/currents within easy access of hands and tools with the covers off and running in either STANDBY or OPERATE modes. Only highly trained personnel completely familiar with this amplifier should attempt this level of servicing.

Safety switches along edges of amplifier rear panel (one on each side) may be overridden if absolutely necessary by pulling the white switch post out until it clicks. The microprocessor power–up tests will then perceive the cabinet as being closed. Note the warning above!

Two safety pressure switches also exist to detect fan failure. if a full STANDBY or OPERATE mode is required for servicing with panels off, these switches may also need to be defeated by placing a shorting jumper across the Pressure Transducer terminals (there are only two terminals).

WARNING:

High voltages (+3KV and +6KV) are fully enabled just as the amplifier enters a STANDBY state.

Section 4.2 Fault Codes

When a fault is detected, UNBLANK is disabled and the amplifier is returned to a safe operating state. In addition, a fault code is displayed in the two 7–segment (numeric) displays on the front of the amplifier and the red FAULT LED is lit.

These codes are intended to help the technician diagnose a problem. In many cases the fault code may only be valuable as a starting place for diagnostics. The actual source of the problem may be “upstream or downstream” of the indicated problem; for example, an MRF134 drain to ground short on the Solid State Amplifier would result in a fault code 21 indicating that the +24 volt supply (Power Control Board) has failed.

Service personnel should consult the schematics in Chapter 5, Service Manual and Section 3.5 of this manual as well as the information contained in this Chapter to locate the root cause of a particular fault code.

The fault codes may be of two general types: fatal and non–fatal. These are defined in Section 4.2.1 along with a complete listing of fault codes in Table 4–1. Probable causes for fault codes are discussed in Section 4.2.2.

Section 4.2.1 Fault Code Listing

Fatal Faults

Fatal faults are conditions that may be unsafe to personnel or the amplifier. If a fatal fault occurs other than in the OFF mode, the amplifier executes an orderly shutdown and returns to the OFF state. The microprocessor prevents the amplifier from again proceeding with its power–up sequence until the internal fault flag is cleared by issuing a “go to off’ command (see Chapter 3). Once the red FAULT LED is off (the numerical code will remain displayed), the amplifier may be again commanded into a power–on mode. If the fault condition is still present, the fatal fault sequence will occur again.

NOTE:

Even though the amplifier is in OFF, a “go to on’ command must be sent to clear the fault flag.

Non–fatal Faults

Non–fatal faults are used to indicate that an illegal command has been issued or an operational irregularity has been detected which does not warrant complete amplifier shutdown. This level of fault does prohibit an OPERATE mode, but returns the amplifier to STANDBY instead of OFF. The internal flag must be cleared by a “return to standby” command (see Chapter 3).

NOTE:

Even though the amplifier is in STANDBY, a “return to standby” command must be sent to clear the fault flag.

Section 4.2.1 Fault Code Listing Continued

Table 4–1 Fault Codes

FAULT	SEVERITY	DESCRIPTION
00	Fatal*	Fault interlock is held in the faulted state (high). The the red FAULT LED does not light for this fault only.
01	Fatal*	EEPROM contains some data inconsistent with a run; watchdog not enabled or motor tune positions not within motor limits.
02	Fatal*	Dual Port RAM problem.
03	Fatal*	A/D on–board 68HC11 has failed.
04	Fatal*	A/D multiplexer has failed.
05	Fatal*	A/D self–test in microprocessor has failed.
06	Fatal*	A stepping motor coil is open.
07	Fatal*	Illegal opcode trade
08	Fatal*	External interrupt high does not cause interrupt.
09	Fatal*	External interrupt low does not cause interrupt.
10	Fatal	Solid State Amplifier thermistor unacceptable.
11	Fatal	SCM cable disconnected or handshake incorrect.
12	Fatal	+100 volt supply unacceptable
13	Fatal	+3KV supply unacceptable.
14	Fatal	IPA tube heater current unacceptable.
15	Fatal	–5 volt supply unacceptable
16	Fatal	+48 volt supply unacceptable.
17	Fatal	+6KV supply unacceptable.
18	Fatal	PA tube heater current unacceptable.
19	Fatal	+32 volt supply unacceptable
20	Fatal	+2.5 volt reference (+5 volt supply) unacceptable
21	Fatal	+24 volt supply unacceptable.
22	Fatal	Motor 1 zero sensor indicates zero continuously.

NOTE:

Fatal* is used for fault codes 00 through 09 to indicate that these faults are a part of the initial microprocessor self test which occurs only when the circuit breaker is first turned on.

(Table 4–1 is continued on the next page)

Section 4.2.1 Fault Code Listing (Continued)

Table 4–1 Fault Codes (Continued)

FAULT	SEVERITY	DESCRIPTION
23	Fatal	Motor 2 zero sensor indicates zero continuously
24	Fatal	Motor 3 zero sensor indicates zero continuously.
25	Fatal	Motor 4 zero sensor indicates zero continuously.
26	Fatal	Motor 1 zero not found.
27	Fatal	Motor 2 zero not found.
28	Fatal	Motor 3 zero not found.
29	Fatal	Motor 4 zero not found.
30		General motor failure.
31		Unused
32	Fatal	Unblank longer than 20.0 milliseconds.
33 34		Unused.
35	Fatal	FET 1 coarse convergence failed.
36	Fatal	FET 2 coarse convergence failed.
37	Fatal	FET 3 coarse convergence failed.
38	Fatal	FET 4 coarse convergence failed.
39 40 41		Unused.
42	Fatal	FET 1 fine convergence failed.
43	Fatal	FET 2 fine convergence failed.
44	Fatal	FET 3 fine convergence failed.
45	Fatal	FET 4 fine convergence failed.
46	Fatal	FET 1 bias tracked out of adjustable range.
47	Fatal	FET 2 bias tracked out of adjustable range.
48	Fatal	FET 3 bias tracked out of adjustable range.
49	Fatal	FET 4 bias was tracked out of range.
50	Fatal	+100 volt supply soft–start failure.
51	Fatal	+100 volt supply run failure.

(Table 4–1 is continued on the next page.)

Section 4.2.1 Fault Code Listing (Continued)

Table 4–1 Fault Codes (Continued)

FAULT	SEVERITY	DESCRIPTION
52	Fatal	IPA tube heater current unacceptable at start.
53	Fatal	PA tube heater unacceptable at start.
54		Unused.
55	Fatal	+3KV unacceptable immediately after soft–start.
56	Fatal	+6KV unacceptable immediately after soft–start.
57	Fatal	+3KV supply soft–start failure.
58	Fatal	+6KV supply soft–start failure.
59	Fatal	+3KV supply or +6KV supply run failure.
60	Nonfatal	IPA AFT does not converge
61	Nonfatal	PA AFT does not converge:
62	Nonfatal	Insufficient power reaching tube output for AFT.
63–69		Unused.
70	Nonfatal	Change mode command while in OPERATE.
71	Nonfatal	Frequency command invalid.
72	Nonfatal	Invalid mode command.
73	Nonfatal	BODY mode forward power too high.
74	Nonfatal	HEAD mode forward power too high.
75	Nonfatal	BODY mode reflected power too high.
76	Nonfatal	HEAD mode reflected power too high.
77	Nonfatal	PA tube grid current too high.
78	Nonfatal	IPA tube grid current too high.
79	Nonfatal	PA tube plate current too high:
80	Nonfatal	IPA tube plate current too high.
81	Fatal	IPA tube arc or +3KV supply arc.
82	Fatal	Cover interlock 1 Son RF Monitor Module) open
83	Fatal	Cover interlock 2 (on AC Switching Module) open.
84	Fatal	RF MON cable disconnected.
85	Fatal	#12 volt externally controlled safety relay not powered.

(Table 4–1 is continued on the next page.)

Section 4.2.1 Fault Code Listing Continued

Table 4–1 Fault Codes (Continued)

FAULT	SEVERITY	DESCRIPTION
86	Fatal	PA tube arc or +6KV
87	Fatal	Arc–detect circuit failure.
88	Fatal	Fan air pressure insufficient.
89	Fatal	Tube air pressure insufficient.
90	Fatal	IPA tube idle DC bias current unacceptable.
91	Fatal	PA tube idle DC bias current unacceptable.
92	Fatal	Line voltage too low.
93	Fatal	Microprocessor “Watchdog” failed to fire in time.
94	Fatal	Microprocessor “Watchdog” intercepted program
95–99		Unused

Section 4.2.2 Fault Code Probable Cause

Each fault code is listed below along with a “probable cause” description. This brief description is intended to provide a quick best estimate of where the source of trouble is likely to be located. It is virtually impossible to list all of the possible causes. Service personnel should utilize the information in this Section only as a good starting place.

00: The fault interlock is being held high. The microprocessor is stuck in reset or the cable between the Processor Board and the Front Panel Display Board has an open.

01: The microprocessor detects a “checksum” error. This generally indicates that the address bus is faulted or the EPROM contains incorrect data; definitely a Processor Board problem.

02: Dual port RAM apparently has failed; a Processor Board failure.

03: A/D samples generated on the Processor Board have failed; a Processor Board failure.

04: A/D multiplexer apparently has failed. Either the Processor Board Board has a problem, or possibly one of the 32 analog convertible signals is unusually errant.

05:A/D on–board self–test has failed; a Processor Board failure.

Section 4.2.2 Fault Code Probable Cause (Continued)

08: Stepping motor coil is apparently open; very possibly an open in the Motor Cavity Cable Harness or connector; less possible cause is a component malfunction on the Processor Board.

07: Illegal opcode trap; a Processor Board failure.

08: External interrupt high does not cause interrupt; a Processor Board failure.

09: External interrupt low does not cause interrupt; a Processor Board failure.

10: Heat sink (Solid State Amplifier) monitor temperature apparently too hot or cold (very unlikely); probably a failed thermistor or loose screw next to thermistor; perhaps a cable problem or Processor Board A/D problem.

11:SCM cable interlock invalid; either the strobe width is too wide, the cable is open, the strobe signal is high impedance, or most likely, the Processor Board has a problem.

12: +100v supply unacceptable; problem could be on the Power Control Board, the Low Voltage Transformer, an AC Switching Module fuse or relay, a bad cable, or a component failure causing excessive loading (including tubes).

13: +3KV supply unacceptable; failure could be on the High Voltage Rectifier/Filter Board (bad capacitors, diode etc.), the 4.5KVA HV Transformer (unlikely), or possibly a bad IPA tube or 7.5 KV capacitor drawing excessive current.

14: IPA tube heater current unacceptable; most likely a bad IPA tube or Power Control Board circuit. Also cabling including feed–thru capacitor is highly suspect.

15: –5 volt supply unacceptable; most likely on the Processor Board. Possibly a bad op–amp on one of the other boards which uses the –5 volt supply.

16: +48 volt supply unacceptable; most likely a bad FET circuit on the Solid State Amplifier Board; possibly a bad Power Control Board circuit or cabling problem.

17: +6KV supply unacceptable is identical to the +3KV supply unacceptable except for the PA tube being a possible cause. Most likely a HV Rectifier/Filter Board problem.

18: PA tube heater current unacceptable; most likely located on the Power Control Board, but very possibly a tube problem. Cabling and feed–thru capacitors are suspect.

19: +32 volt supply unacceptable; most probable sources of trouble are the AC Switching Module (fuses or transformer T1), the Power Control Board, Motors, and cabling.

20: +2.5 volt reference unacceptable; most likely a failure on the Processor Board or the AC Switching Module transformer T1 or fuses.

Section 4.2.2 Fault Code Probable Cause (Continued)

21: +24 volt supply unacceptable; this may arise from any of the supply's numerous loads: Solid State Amplifier, Power Control Board, Processor Board, RF Monitor Module, AC Switching Module, and PA Input Board.

22–25: Motor 1, 2, 3, or 4 zero sensor fault; this either Indicates motor is stuck at zero, its optical sensor is stuck open, AFT forced the motor into the zero stop, or cabling has failed.

26–29: Motor 1, 2, 3, or 4 zero not found; possibly a problem with motor diver chips on the Processor Board. Most likely a failed motor assembly: zero sensor, stuck washers,or cabling.

30: General motor fault; one or more of the four motors suddenly (by the microprocessor's perception) no longer has the correct number of steps or the has a changed zero position. This most likely indicates a motor assembly failure (usually stuck counter washers); possibly a driver failure on the Processor Board.

31: Unused.

32: UNBLANK longer than 20 milliseconds; either the UNBLANK signal generated by external equipment is too long, or the Processor Board has a problem.

33–34: Unused.

35–38: FET 1, 2, 3, or 4 coarse convergence failure; a problem with either the Solid State Amplifier Board (most likely), the Processor Board, or cabling in between.

39–41: Unused.

42–45: FET 1, 2, 3, or 4 fine convergence failure; identical to faults 35–38 probable cause.

46–49: FET 1, 2, 3, or 4 tracked out of adjustable range; this problem is identical in probable cause to faults 35–38 except that an even higher probability exists for the failure to exist on the Solid State Amplifier Board.

50: +100 volt supply soft–start failure; this early failure of the +100 volt supply is probably due to an excessive load by one of the tubes or a circuitry failure on the Power Control Board. It is also very possible that a problem exists in the AC Switching Module relays or fuses; perhaps a failed Low Voltage Transformer (not very likely).

51: +100 volt supply run failure; identical to fault 50 probable cause.

52: IPA tube heater current unacceptable at start; identical to fault 14 probable cause.

53: PA heater current unacceptable at start; identical to fault 18 probable cause.

Section 4.2.2 Fault Code Probable Cause (Continued)

54: Unused.

55: +3KV supply unacceptable immediately after soft–start; this failure is most likely due to a problem in the High Voltage Rectifier/Filter Board, and very possibly a relay problem in the AC Switching Module. Other sources of the failure could be the 4.5KVA HV Transformer, loading in the VTAC, and bad A/D on the Processor Board.

58: +6KV supply unacceptable immediately after soft–start; identical to fault 55 probable cause.

57: +3KV soft–start failure; differs from fault 55 only in timing.

58: +6KV soft–start failure; identical to fault 56 except for timing.

59: +3KV supply or +6KV supply run failure; shares the same probable causes as faults 55 through 58.

50: IPA AFT does not converge; this indicates that sufficient power exists for AFT but the motors cannot force a zero–phase condition. Problems could exist with the motors, motor drivers, IPA phase detector, Processor Board A/D, IPA tube, or cabling.

61: PA AFT does not converge; identical to fault 60 probable cause.

62: Insufficient power reaching tube output for AFT; most likely this problem is due the Solid State Amplifier oscillator or path switching. Also very likely is a bad connection between Solid State Amplifier and the VTAC. Other potential sources of failure could be the IPA tube, IPA input board, IPA phase detector, Processor Board A/D, and cabling.

53–89: Unused.

70: Change mode command while in operate; if no such command is being issued by the external controlllng computer, then the Processor Board is definitely at fault.

71: Frequency command fault; if the frequency command byte is correct, then the Processor Board is the failure.

72: Invalid mode command; identical to fault 70 probable cause.

73: BODY mode forward power too high; if the RF input power to the amplifier is normal, the the failure is most likely in the RF Monitor Module. Possibly the Processor Board A/D has a problem.

74: HEAD mode forward power too high; identical to fault 73 probable cause.

75: BODY mode reflected power too high; if the amplifier load is normal, then the probable cause is the same as for fault 73.

76: HEAD mode reflected power too high; identical to fault 75 probable cause.

Section 4.2.2 Fault Code Probable Cause (Continued)

77: PA tube grid current too high; most likely an indication that the YC–156 tube is failing. Possible problems on the Power Control Board or Processor Board.

78: IPA tube grid current too high; identical to fault 77 probable cause.

79: PA tube plate current too high; the probable causes are the same as for fault 77 except that the High Voltage Rectifier/Filter Board is also suspect.

80: IPA tube plate current too high; identical to fault 79 probable cause.

81: IPA tube or +3KV arc; a genuine arc will usually leave a visible mark, and will most probably eventually occur again. Tube arcs may occur internally and will not be visible; if these persist, the tube must be replaced. it is also possible that the arc detect circuitry on the Processor Board is giving false indications.

82: Cover interlock 1 (on RF Monitor Module) open; if the Motor Cavity Right Side Cover is in place, then the switch has failed, a cable is open, or Processor Board has failed.

83: Cover interlock 2 (on AC Switching Module) open; identical to fault 82.

84: RF MON cable disconnected; if RF MON cable is correct, then failure is on the Processor Board.

85: Externally controlled +12 volt safety relay not powered; if the RF MON cable is correctly supplying the voltage, then the Processor Board has a problem.

86: PA tube or +6KV arc; identical to fault 81, but with more punch.

87: Arc detect circuit failure; a Processor Board failure.

88: Fan air pressure insufficient; if the fans are turning and the covers are on, then either the pressure transducer has failed, cabling has failed, or an A/D problem exists on the Processor Board (unlikely).

89: Tube air pressure insufficient; identical to fault 88 probable cause.

90: IPA tube idle DC bias current unacceptable; either the tube or the Power Control Board has failed. Possibly a cable, IPA Input Board, or Processor Board A/D problem.

91: PA tube idle DC bias current unacceptable; identical to fault 90.

92: Line voltage too low; if line voltage is always greater than 180 volts, then Processor Board or AC Switching Module has a problem.

93: Microprocessor “Watchdog” failed to fire in time; a Processor Board failure.

94: Microprocessor “Watchdog” intercepted program; a Processor Board failure.

95–99: Unused.

Section 4.3 Fuse Bank

This Section contains a list of all fuse functions and ratings. All replaceable fuses are located in the fuse bank on the rear upper right corner of the amplifier (see Figure 1–1, Chapter 1). These fuses are actually a part of the AC Switching Module; schematic 86–013–2110 is useful for information supplemental to this Section.

It is usually a good idea to begin diagnostics with a check of fuses that may directly correspond to a particular fault, as well as all fuses that may be "upstream" of a particular fault (consult amplifier background testing chronology in Chapter 3).

NOTE:

All fuses are of type 3AG 250 volt SB (slow blow).

Table 4–2 Fuses

FUSE	RATING	FUNCTION
F1	2 amps	Current limit for secondary of AC Switching Module transformer T1 supplying Processor Board
F2	2 amps	Current limit for secondary of T1 (same as F1)
F3	1 amp	Current limit for primary of AC Switching Module transformer T1
F4	1/2 amp	Current limit for BLOWER PHASE1, Blower Assembly
F5	1/2 amp	Current limit for BLOWER PHASE2, Blower Assembly
F6	1 amp	Current limit for primary of AC Switching Module transformer T1.
F7	1 amp	Current limit for FAN PHASE1, air intake fans.
F8	1 amp	Current Limit for FAN PHASE2, air intake fans.
F9	2 amps	Current limit for +32 volt supply.
F10	2 amps	Current limit for 208V P1A primary of Low Voltage Transformer supplying Power Control Board.
F11	2 amps	Current Limit for 208V P1 C primary of Low Voltage Transformer.
F12	2 amps	Current limit for 208V P1 B primary of Low Voltage Transformer.

Section 4.4 Circuit Test Points and Factory Adjustments

As an aid to diagnostics and initial factory calibration, several test points have been built into the circuit boards. These points consist of raised metal loops labeled TPx where x is a number. The metal loops allow for easy attachment of test clips. Exact locations of test points and their interconnection within the circuits are to be found in the schematics in Chapter 5, Service Manual.

Test points exist on three of the amplifier modules: Processor Board, Solid State Amplifier Board, and the Power Control Board. Test points and adjustments for each of these boards and the adjustments required on the IPA Input Board are discussed in the next four Sections.

Section 4.4.1 Processor Board Test Points

Processor Board Test Points

All test points and jumper pins provided on the Processor Board are fully described in Table 4–3.

Table 4–3 Processor Board Test Points and Jumpers

POINT	SIGNAL	DESCRIPTION
TP1	AS (Address Strobe)	Provides quick verification of microprocessor mode. This test point should be a 2MHz square wave, about 25% duty for expanded multiplex address mode.
TP2	RESET	Logic low indicates the microprocessor is in reset.
TP3	Ground	Tied directly to ground on the Processor Board.
TP4	32V RET	Return line (ground reference on Power Control Board) of +32 volt supply
TP5	+32V	Positive side of +32 volt supply originating from Power Control Board.
TP6	+24S	+24 volt supply originating from Power Control Board; switched in line with relay powered exteranlly through RF MON cable (12 volt safety relay)
TP7	+24V	+24 volt supply from Power Control Board.
TP8	+5VR	Regulated +5 volt supply,; powers almost all logic.
TP9	–5V	Regulated minus 5 volt supply

(Table 4–3 is continued on the next page.)

Section 4.4.1 Processor Board Test Points (Continued)

Table 4–3 Processor Board Test Points and Jumpers (Continued)

POINT	SIGNAL	DESCRIPTION
W1	BISYCL BICYCLE	BISYCL and BICYCLE SCM communications modes; BISYCL is the factory default. This jumper must be paired identically with the W2 jumper.
W2	BISYCL BICYCLE	Identical to W1 jumper; the two jumpers must be configured identically
W3	RESET MODA MODB	Five pin jumper used to configure the 68HC11 operating mode. Factory default is all pins open for expanded multiplex mode.

Processor Board Factory Adjustments

There is only one factory adjustment made on the Processor Board.

1. **+5 volt supply.** Adjust potentiometer R122 until 5.00 volts is obtained at test point TP8.

Section 4.4.2 Solid State Amplifier Test Points

Solid State Amplifier Test Points

All test points and jumper pins provided on the Solid State Amplifier Board are fully described in Table 4–4.

Table 4–4 SS Amplifier Test Points and Jumpers

POINT	SIGNAL	DESCRIPTION
TP1	1341 +	+24 volt supply; used for MRF134 FET bias.
TP2	1341–	+24 volt supply after 0.1 ohm resistor used to sense supply current (1 millivolt = 10 milliamps). TP1 and TP2 are used for MRF134 manual bias.
TP3	FET BIAS	Output of current to voltage to transducer utilized by the microprocessor to set and maintain MRF148 and MRF150 FET bias,; 255 milliamps per volt.

(Table 4–4 is continued on the next page.)

Section 4.4.2 Solid State Amplifier Test Points (Continued)

Table 4–4 SS Amplifier Test Points and Jumpers (Continued)

POINT	SIGNAL	DESCRIPTION
W1	UNBLK	Forces UNBLANK on the SS Amplifier to enable the +24 volt supply for biasing the MRF 134 FETs.
W2	Q23 BIAS OFF	Shorts O23 gate voltage to ground so that Q24 bias may be independently set utilizing TP1 and TP2.
W3	Q24 BIAS OFF	The complement of the W2 jumper; shorts O24 gate bias so that O23 may be independently set.

Solid State Amplifier Factory Adjustments

1. **Oscillator power.** Configure Solid State Amplifier Board for oscillator to TEST RF OUT port using the serial “A” command: “ADO”.

   Measure power and frequency at the TEST port (J2504) on the rear panel and adjust the variable inductor L1 for maximum stable output power (upper mid–range).

   CAUTION:

   Power levels in excess of 15 dBm (30 milliwatts) may be available at the TEST port during this process. Be sure that the measuring device is capable of withstanding this power, or attenuate the signal to a safe level.

2. **Set MRF134 DC drain current bias levels to 225 milliamps.** Place amplifier in OFF mode with Solid State Amplifier Board installed.

   Turn potentiometers R121 and R124 fully counter–clockwise to ensure initial zero voltage on the FET gates.

   Place jumper across W2 to short bias voltage on FET O23. Place jumper on W1 to “UNBLANK” the +24 volt supply.

   Connect voltmeter capable of accurately measuring millivolts across test points TP1 and TP2 and adjust potentiometer R 124 until a voltage of 22.5 millivolts exists across TP1 and TP2.

   Move the jumper from W2 to W3 and repeat adjustment on potentiometer R121 as done for R124 to set O24 bias such that 22.5 millivolts exists across TP1 and TP2.

Section 4.4.3 IPA Input Board Test Points

IPA Input Board Test Points

There are no test points provided on this board.

IPA Input Board Factory Adjustments

1. IPA Input tune. Set up amplifier to measure forward and reflected power for Solid State Amplifier feeding into the VTAC (connector IPA RF IN) using a four port directional coupler.

   Adjust “pi” tuning–circuit capacitors TUNE and LOAD for less than 40 dB of reflected power.
2. IPA Phase Adjustment. Set up amplifier to measure its bandwidth centered about 63.860 MHz.

   Adjust IPA PHASE capacitor so that HEAD mode bandwidth is consistently centered after executing AFT.

Section 4.4.4 Power Control Board Test Points

Power Control Board Test Points

All test points and jumpers on the Power Control Board are fully described in Table 4–5.

Table 4–5 Power Control Board Test Points and Jumpers

POINT	SIGNAL	DESCRIPTION
TP1	+48V	Tied to the +48 volt supply
TP2	PA HTR–	The “negative” output line of the floating 15.2 volt PA tube heater supply (floats on the PA tube cathode potential).
TP3	PA HTR +	The “positive” output line of the PA heater supply
TP4	IPA HTR +	IPA tube heater supply
TP5	IPA CATHODE	IPA tube cathode to grid bias potential.
TP6	PA CATHODE	PA tube cathode to grid bias potential.
TP7	+24V	Tied to the +24 volt supply
TP8	GROUND	Tied to Power Control Board around reference.

Section 4.4.4 Power Control Board Test Points(Continued)

Power Control Board Factory Adjustments

1. + 24 volt supply. Set potentiometer RB4 to ten turns from fully counter–clockwise position.

   Enable the U10 voltage regulator by setting FLT 3 high and adjust potentiometer R92 until +24.00 volts is obtained at test point TP7.

   Load supply to 2.2 amps and adjust pot RB4 to set current limit to 2.2 amps.

2. IPA tube heater supply. Enable tube heater supply by setting /ENABLE line low.

   Adjust potentiometer R108 for 15.2 volts at test point TP4.

3. +48 volt supply. Enable the U1 voltage regulator by setting the /ENABLE line low.

   Adjust potentiometer R10 until 48.00 volts is obtained at test point TP1.

4. PA tube heater supply. Enable the tube heater supply by setting/ENABLE line low.

   Adjust potentiometer R41 until 15.2 volts is obtained across test points TP3 and TP4.

Section 4.5 RF Signal Path Diagnostics

The RF path through the amplifier may be broken down into essentially three subsections as described in Section 2.1 of Chapter 2. RF power enters at the Solid State Amplifier (SS Amp), exits at about 80 or 160 watts (nominal BODY or HEAD output with 0.4 milliwatts input), and then enters the vacuum tube amplifier cavity (VTAC) where it is amplified by another 11 or 24 dB. Finally, the RF signal passes through the RF Monitor Module to detect forward and reflected power levels.

This modularity greatly simplifies diagnostics of RF signal path troubles since the signal may be independently measured at each of these three subsections. This quickly narrows the problem down to a single subsection.

This RF diagnostics discussion is orientated towards the three subsection modularity just described; the Solid State Amplifier and the VTAC subsections are discussed separately in the next two Sections; the RF Monitor Module is addressed within the VTAC discussion.

Section 4.5.1 Solid State Amplifier Diagnostics

Pulsed RF enters the SS Amp through connector J2503 RF IN. This connector physically resides on the Solid State Ampiifier Board 86–013–2500. RF input is 50 ohm characteristic impedance and designed for –4 dBm (+/– 4 dB) input to produce maximum output power in any mode.

The procedures described in this Section enable the identification of a faulty SS Amp Board, and locates essentially where on the board the problem lies. The diagnostics and trouble shooting are designed towards module replacement. Therefore, once an SS Amp is diagnosed as faulty, it should be replaced with a new one. Refer to the Service Manual for ordering and replacement procedures.

Insufficient Output Power

The most common problem associated with the SS Amp is insufficient power reaching the VTAC. Many things can cause this problem. The first step is to make certain that the SS Amp is the actual failure. If there is insufficient power in both the HEAD and BODY modes, then the SS Amp is very possibly at fault.

There are numerous other potential sources of this kind of trouble in the VTAC and the RF Monitor Module also. And it may even be possible that the Processor Board has configured the RF paths or bias currents incorrectly. The first step is to measure the SS Amp output power.

Checking SS Amp Output Power

This procedure requires removal of the Motor Cavity Right Side Cover and defeating the cover interlock switch in the RF Monitor Module. See Section 4.1 for details and cautions.

Begin at the RF IN J2503 connector and measure the RF input power at the RF IN (J2503) connector. Use a standard MR pulse (sinc, square, or ramp) with a peak power level of about –4 dBm, about 3 to 5 miliisecond pulsewidth, and five percent duty cycle. Connect a 50 ohm, 30 dB, 200 Watt through–line attenuator (or rough equivalent) to output connector P2505 of the SS Amp. Connect an osciiloscope (with 50 ohm input) to the other end of the attenuator.

A 50 ohm terminator should also be connected to the IPA RF IN J2601 connector feeding the VTAC. This ensures that a runaway oscillation will not occur in the tube cavity when the amplifier is brought into OPERATE without the SS Amp connected.

Bring the amplifier into HEAD and OPERATE modes. Measure the peak output power (oscilloscope voltage) from the SS Amp. In HEAD mode, the normal range of output power is between 126 and 200 Watts (51 and 53 dBm) for – 4 dBm input. Therefore, a power level of approximately 160 mW should be present at the input of the oscilloscope for 30 dB of attenuation (approximately 4 volts peak in 50 ohm system).

Section 4.5.1 Solid State Amplifier Diagnostics (Continued)

Repeat the power output measurement for the BODY mode. The normal output power of the SS Amp is between 63 and 100 Watts (48 to 50 dBm) for –4 dBm input. The power to the oscilloscope should be about 80 mW (about 2.8 volts peak).

If only one mode's maximum output power is correct, there is high probability that the step attenuator portion of the SS Amp has failed (or possibly the digital control). Proceed with the Step Anenuator Check–out beiow.

RF Path Through 30 dB Gain Block

The SS Amp RF path can be subdivided into two blocks by looking at power out of the TEST RF OUT port J2504. The RF path to this port includes the input connector (J2503), step attenuators, signal routing diode switches (EXTOUT, INTRF, EXTRF), and a 30 dB integrated circuit gain block (A1).

Connect 30 dB through–line attenuator and 50 ohm oscilloscope to the TEST RF OUT connector. Put the amplifier into TEST and OPERATE modes. Power out should be between 50 and 80 mW (17 to 19 dBm) for an input power of 4 dBm. Therefore, a power of about 63 microwatts should be input to the oscilloscope (79 millivolts peak for 50 ohm system).

If the power out this port is correct, but the total SS Amp power out is wrong (at P2505), the problem is in the FET gain stages (O23–O28) or associated circuitry, and the SS Amp should be replaced; although there is still a small (very) possibility of a Processor Board failure setting the FET bias currents incorrectly.

If there is no power out at J2504, then use the oscilloscope to trace the signal to the failure. Observe RF input at the junction of R102 and R103, which is the signal path immediately after the RF input. If there is no RF present here, J2503 is probably open or shorted. Next, look at pins 1, and then 9, of A1 (the IC gain block). A significant gain in the RF envelope should be seen between these two pins. These two measurements will narrow down a complete power failure to the gain block, just after it, or between J2504 and the gain block

No power out of the TEST port could also be a symptom of digital control probiems. This may be component failure on the SS Amp board (signal routing PIN switches or logic ICs), or Processor Board problems. A storage oscilloscope can be used to check digital signal flow. The Step Attenuator and Osciliator sections below also give a good indication if digital control is working.

If there is power out, but the power–out level is incorrect, the most likely problem is the step attenuators, or a weak gain block, or even a PIN diode switch with high insertion loss. Proceed to the Step Attenuator Check–out section for further diagnostics.

Section 4.5.1 Solid State Amplifier Diagnostics (Continued)

Step Attenuator Check Out

A convenient method of checking the step attenuator is to use the internal oscillator as a driver to the TEST RF OUT port. It is assumed here that the oscillator is working, since it is only used for automatic fine tuning purposes. AFT problems could cause insufficient overall amplifier output power, but the SS Amp would still output its full power. It is unlikeiy that both the attenuator and oscillator would fail at the same time (unless digital control has failed).

Put the amplifier into an OFF mode (keep circuit breaker switch on). Disconnect power input to connector J2503 (RF IN), and connect the 30 dB through–line attenuator and 50 ohm oscilloscope (as discussed in the Insufficient Output Power section above) to TEST RF OUT (J2504).

First verify oscillator power. The oscillator is turned on with the serial command listed below (see Chapter 3). This command as given also sets the step attenuator to zero for full oscillator output power.

Execute serial command “ADO” to enable oscillator and set step attenuator to zero.

NOTE:
In the OFF mode, the serial “A” command must be enabled by manually putting the GATE (pin 13) of U9 to ground to enable the output latch.

The output power shouid lie in the range of 10 to 30 mW (10 to 15 dBm); therefore, a nominal power of about 15 microwatts (39 millivolts in 50 ohm system) should be input to the oscilioscope after the attenuator. If the oscilloscope can handle the full power of the oscillator (50 milliwatts or better capability), better resolution will be provided by feeding the TEST RF OUT port directly into the scope.

If no power is output, use the oscilloscope to view oscillator RF at the junction of R94 and R95. Note that the osciliator is forced on by tying the “far” side of R50 to +5 volts.

Step through the attenuator by serially writing “AD1 ”, “AD2”, and so on to “ADF”. The last step (ADF) is the maximum attenuation of approximately 22.5 dB. The attenuation steps are on the order of 1.5 dB per increment (+/– 0.5 dB), which is equivalent to a 29 percent decrease in power (16 percent decrease in voltage) per step.

If the step attenuator can be sequentially stepped, serial communications is working properly. If any attenuator step is grossly out of range, this is a possible cause of low (or possibly high) power output in HEAD and BODY modes. If serial communications is working, and the attenuator steps are all in range, signal loss is likely due to some path attenuation (PIN switch with insertion loss, short), or a weak gain block. It should be safe to assume that the Processor Board is functioning properly; so replace the SS Amp.

Reset the amplifier when finished with the “A” command by turning the main circuit breaker (on the rear of amplifier) off and on again. Remember to unground pin 13 of U9.

Section 4.5.1 Solid State Amplifier Diagnostics (Continued)

FET RF Path Failure Or Convergence Faults

The procedures in this section can be used to determine if the FETs (or associated circuitry) have failed. The failure may be in the form of either insufficient power or an FET convergence fault (course or fine).

An FET convergence fault wili be issued by the microprocessor if the coarse and fine DACs reach full scaie without producing sufficient (target in EEPROM) bias current. If fault code 38, FET 4 coarse convergence failure, occurs, first check the current transducer as discussed next. Otherwise, skip the next two paragraphs.

Put the amplifier in OFF mode, and attach a 50 ohm resistor (50 watts minimum!) between FB2 or FB3 (the 48 volt bus) and ground (negative side of C18 is a convenient ground ciip point). Issue a “go to standby” command (Chapter 3), and observe the voltage at test point TP3 which is the voltage output of the FET bias current transducer.This must be done before STANDBY is reached. The 50 ohm resistor should draw 0.96 amps, thus producing 3.76 volts at TP3 if the current transducer is working (0.0039 volts per milliamp of +48 volt supply current). Check that +48 volts is present at FB2 or FB3 before doing this test (+48 volt supply comes up during OFF to STANDBY delay).

If the voltage at TP3 is correct, proceed to the next paragraph. Otherwise, check for +48 volts on both sides of R33 to confirm R33 is still functional. Note that diode D19 is parallel with R33 to protect the resistor from +48 volt supply ground shorts. If the voltage across both sides of R33 is a diode drop (0.5 to 0.8) volts, then R33 is open; replace the Solid State Amplifier Board.

If the current transducer is functioning properly, then usually (about 75 percent of the time) a coarae convergence failure (faults 35–38) occurs for an FET other than FET 4. Then either the FET has failed or the coarse adjust bias circuitry for the FET has failed; replace the SS Amp.

An FET fine convergence failure (faults 42–45) or bias tracked out of adjustable range (faults 46–49) could possibly be due to a failure of the fine DACs on the Processor Board (or A/D may have failed, perhaps cabling). Most likely the failure is on the SS Amp. Check the fine DACs on the Processor Board for reasonable output. It may be useful to read the RAM Address Codes (Chapter 3) for the coarse and fine DACs to see if reasonable values in agreement with measurements are present.

Oscillator/AFT Circuit

The SS Amp on–board oscillator supplies the signsl used for AFT purposes. If the oscillator fails, improper AFT will occur, and insufficient output power and skewed bandwidth may result. If AFT problems are suspected, first check the oscillator function and output power with the procedure described in the Step Attenuator Check Out section above.

Section 4.5.1 Solid State Amplifier Diagnostics (Continued)

If the oscillator is functioning properly, then check for a pulse train exiting the SS Amp output P2505 during AFT (which occurs just as going into OPERATE). Note that AFT must be enabled (see Chapter 3).

The output power (measured in the same way as described for the Checking SS Amp Output Power section) should nominally be 25 Watts (44 dBm +/– 4 dB) in either HEAD or BODY mode.

If the osciilator is functioning and a pulse train is exiting the SS Amp, then the SS Amp is not the problem. Otherwise, the SS Amp is most likely the problem. Check that the step attenuator is functioning to verify Processor Board digital communications before replacing the SS Amp.

Section 4.5.2 Vacuum Tube Amplifier Cavity Diagnostics

General Notes

It is important to remember that if any of the four motor driven capacitors are disturbed (rotated) by hand, the microprocessor will lose track of their positions. To reset the capacitors refer to the “Z” command as described in Chapter 3. Also, cycling the circuit breaker off and on will cause the amplifier to re–zero the motors as a part of its normal OFF to STANDBY function.

The two vacuum tube stages are normally run “open loop” meaning that there is no intentional RF or envelope feedback path within the amplifier. During AFT a form of feedback is used; the two phase detector outputs are driven to a “zero voltage condition” (nominally 2.5 volts) by iteratively stepping the “TUNE” capacitors to center the passband of the tuned circuits.

A phase detector false zero voltage condition can occur if the crystal oscillator section of the Solid State Amplifier Board has failed resulting in no output power to the internal load during AFT. If this condition occurs, power output during normal SIGNA operations may be below normal or even above normal, and the amplifier passband is likely to be skewed.

This Section is organized in a block format addressing “modes” of failure. Consult the most applicable subsection below for the symptoms present.

No BODY output or low BODY output, HEAD output normal.

Connect through–line attenuator(s) of 60 dB to J2804 (BODY output) on the RF Monitor Module. Connect a 50 ohm oscilloscope to the output of the attenuator. Synchronize the scope via its external trigger capability to the UNBLANK signal. Put the bandwidth limit control on the oscilloscope to off.

Section 4.5.2 Vacuum Tube Amplifier Cavity Diagnostics (Continued)

Place amplifier in BODY and OPERATE modes, and inject –4 dBm of gated drive at 63.860 MHz from the SIGNA system or other equipment into the amplifier's RF input connector (J2503). A 3 millisecond wide RF pulse repeated every 60 milliseconds (or more) is suggested.

The power to the oscilloscope should be about 20 milliwatts (13 dBm) which corresponds to about 1.4 volts peak for a 50 ohm system. If scope reading is within about 10% of desired value, the amplifier is probably functioning normally. The SIGNA output cable/connector in the amplifier rack may be defective, or the amplifier may be saturating prematurely (most likely poor tune or weak PA tube).

To check for saturation, lower and then raise the RF input by a few 1 dB increments. If the scope deflection changes by about 11% per increment, the amplifier is not saturating. Otherwise, the amplifier is saturating; perform the PA Phase Detector diagnostics below before changing the PA tube.

If the amplifier is responsible for the low BODY power (as deduced from above), remove the RF drive and bypass the RF Monitor by connecting the 60 dB through–line attenuator directly to the VTAC BODY output (J2603). This requires removal of the Motor Cavity Right Side Cover and defeating the cover interiock switch in the RF Monitor (see Section 4.1). Re–apply the RF input drive and measure the output power. If scope voltage readings are now correct (as defined above), replace the RF Monitor Module.

If direct BODY output is still low, then the PA tube, perhaps one of the power supplies (+6 KV, + 100 V, or PA tube heater), or the RF relay K1 on the PA input board are the most probable causes. Gross mistuning due to a bad PA phase detector is less likely but should be checked before attempting a tube change.

Refer to the power supply section (Section 4.7) for diagnosing possible problems with the +6KV supply, the + 100 volt supply, and the PA tube heater supply.

RF Relay on PA input Board

If the BODY output is very low at VTAC J2603 connector (50 mV peak or less at 50 ohm oscilloscope after 60 dB attenuator), vacuum relay K1 is probably not energized. This can be caused by either an open coil or a faulty relay driver.

Open the Left Side Cover and defeat the cover interlock switch in the AC Switching Module (see Section 4.1). Measure the DC voltage between feed–through capacitors C13 and C14 on the Processor Cavity bulkhead (marked +24V and RF RLY1). A reading significantly less than 23 volts (BODY mode) indicates that the driver (on the Processor Board) has failed (or relay coil has possibly shorted).

To test the relay coil, turn the amplifier completely off and measure the resistance between the same two capacitors. If the resistance is markedly higher or lower than 330 ohms (e.g. several kilo ohms or near zero), replace the PA Input Board.

Section 4.5.2 Vacuum Tube Amplifier Cavity Diagnostics (Continued)

PA Phase Detector

A simple test can be performed to determine if the PA Phase Detector is causing the amplifier to be grossly mistuned. Connect a 10:1 high impedance probe to a second vertical channel of the oscilioscope and set the scope to display 1 volt DC per division. Connect the scope to pin 15 of resistor pack RP148 on the Processor Board and chassis ground. Turn scope bandwidth limit “on.”

Inject a –4 dBm signal into the amplifier as before and observe the oscilloscope. The steady state level during the time that the amplifier is BLANKed (i.e. no RF) should be somewhere near 2.5 volts DC (the “zero phase” condition). During UNBLANK (with RF pulse), the level should be within +/– 1 volt of the zero phase condition (2.5 volts). Slowly rotate motor shaft of MOTOR 3 by hand in both directions from it’s initial value. The phase detector output voltage should swing about +/– 2 volts to either side of the zero phase condition.

If the phase detector voltage remains permanently at one of the limits then check the SMA connectors on the PA Phase Detect Assembly for tightness; replace assembly if loose connectors are not the cause.

If the above diagnostics are inconclusive, perform the Amplifier Tuning and AFT diagnostic procedures in Section 4.6. The PA tube should only be replaced after all other tests pass. Refer to the tube changing instructions in the Service Manual.

BODY output normal, HEAD output low.

This condition should be easily traceable to one of three possible causes. First connect the 60 dB through–line attenuator and 50 ohm oscilloscope to the HEAD output port (J2803) as described above for HEAD normal, BODY low power diagnostic. Put the amplifier in HEAD and OPERATE, and apply –4 dBm of RF drive also as discussed above. The power into the oscilioscope should be about 2 milliwatts (3 dBm) which should be about 0.445 volts peak on the oscilloscope. If somewhere near this level is achieved, the SIGNA output cable/connector in the rack is probably defective.

Otherwise, bypass the RF monitor by connecting the attenuator/scope directly to P2602 connector on the VTAC. This requires removal of the Motor Cavity Right Side Cover and defeating the cover interlock switch in the RF Monitor (see Section 4.1). If the output power is now found to be correct, replace the RF Monitor Module.

The third possible cause is that RF relay K1 on the PA Input Board is stuck in the BODY position due to either mechanical failure, or a bad relay driver on the Processor Board. This situation would give a very low voltage swing on the oscilloscope (3 millivolts peak or less). The relay coil voltage should be zero volts as measured (HEAD mode) between feed–through capacitors C13 and C14 (marked +24V and RF RLY1 in the Processor Cavity). Replace the Processor Board if the relay is being energized (relay should only be energized in BODY mode). Otherwise, replace the PA Input Board since the relay being stuck is the only way for BODY output to be normal and HEAD output very low.

Section 4.5.2 Vacuum Tube Amplifier Cavity Diagnostics (Continued)

BODY output low, HEAD output low.

There are two primary possible causes of this condition: a defective IPA amplification stage or a defective Solid State Amplifier Board. Refer to Section 4.5.1 and determine if the output power reaching IPA RF IN connector J2601 from the Solid State Amplifier is within specifications.

After the correct Solid State Amplifier power has been established, put the amplifier in the HEAD and OPERATE modes, inject a 4 dBm signal into the amplifier, and set up the 60 dB through–line attenuator and 50 ohm oscilloscope as discussed in the HEAD Low, BODY Normal section above. First connect the 60 dB attenuator to the RF Monitor HEAD output (J2803) and then to the VTAC IPA RF output (J2602) to measure output power. Scope bandwidth limit should be off. The VTAC output measurement requires that the Motor Cavity Right Side Cover be removed and the cover interlock switch be defeated (see Section 4.1).

If a significant increase in output level is observed by bypassing the RF Monitor Module, replace it. The power into the oscilloscope should be about 2 milliwatts (3 dBm) which corresponds to about 0.445 volts peak in a 50 ohm system.

If the output power is still low at the VTAC output (J2602), check all IPA power supply voltages as discussed in Section 4.7 (IPA tube heater, +32 volt supply, and +3KV supply).

The remaining possible causes for low power in both modes are a bad (or misadjusted) VTAC IPA Input Board including mistuning due to a faulty IPA phase detector section, or a weak 3CPX800A7 tube.

Perform the Amplifier Tuning and AFT diagnostics in Section 4.6 to attempt to confirm proper tuning. Also, the PA Phase Detector procedure described on the previous page may be replicated for the IPA phase detect circuitry by looking at pin 1 of RP14B on the Processor Board and manually moving the shaft of MOTOR 2. This is useful if enough power is present to excite the detector (2.5 volts nominal should always be true during BLANKed periods).

If the IPA Input Board and the IPA tube are still both suspect, insert a known good tube (if possible) before changing the IPA Input Board. If the tube is permanently changed, refer to the tube retuning procedures the Service Manual.

NOTE:
Prior to commifting to an IPA input board change it may be worthwhile to check the tightness of the backnut on the BNC input connector J2601.

Section 4.5.2 Vacuum Tube Amplifier Cavity Diagnostics (Continued)

High Voltage Arcs and Tube Arcs

A fault 81 or 86 simply means that the fault monitor has detected excessive current flow which is usually associated with an arc somewhere in the high voltage circuits (+3 KV or +6 KV). A true tube arc (within a tube) is essentially inaudible due to the tube vacuum. An external arc, which is clearly audible, can be caused by arcing over a dirty tube or more probably one of the 7.5 KV ceramic capacitors within the VTAC.

Since the IPA uses the same 7.5 KV capacitors as the PA, and is run at half the voltage, an arc in this stage is not nearly as likely. There are 7 capacitors within the PA stage that could produce this fault condition. Three are mounted between the PA anode strap and sheet metal inductor L10 (C8–C10); one is mounted on the amplifier top cover (C5), and three (C1–C3) are part of the VTAC Filter Board mounted on the bulkhead.

Low voltage resistance tests of the capacitors will not normally be adequate to detect a failed capacitor. The simplest approach to locating the source of an arc is a process of eiimination by isolating certain capacitors from the circuit and placing the amplifier in STANDBY (this brings up the high voltage).

Start by disconnecting the PA anode RF choke (L9) at the tube anode, which will remove CB–C10 (and PA tube) from the HV path, and bring the amplifier to STANDBY. These three capacitors are the most likely source of external arcs. If an arc occurs, remove C5 and repeat. The only capacitors left are those on the VTAC Filter Board. Also, external arcs (with respect to tube) usually leave some trace such as black burn marks or small welds. Make a thorough visual inspection of the tube cavities.

WARNING:
Always turn off the amplifier main power and short all contacted VTAC areas to ground before touching; the high voltage capacitor bank can retain a significant charge. Always replace the VTAC Right Side Cover when turning amplifier power back on.

Section 4.6 Processor Board Diagnostics

General Notes

A problem on the Processor Board cannot (in general) be diagnosed by using the SCM control port alone. It is usually necessary to connect an RS–232 terminal (Data General, Boot Terminal) or a computer configured for 9600 baud, 1 start bit, 8 data bits, and 1 stop bit. An oscilloscope (preferably a storage scope) wili also be needed. Access to the Processor Board is gained from the Processor Cavity with the AC Switching Module lowered to expose the board.

It will be most helpful to have read Chapter 2, Section 2.2 on Processor Board theory. The Chapter 3 discussion of microprocessor firmware, addresses, and commands will also be referenced frequently.

General Diagnostics

The first step in determining if the Processor Board is faulty is to establish serial communications with the on–board 68HC1 1 microprocessor. Connect the serial terminal and cycle the amplifier's main circuit breaker off and then on. The "hello" message should appear on the serial terminal. This message is a string of characters sent at the completion of the self test (fault codes 00–09). If a fault code 00–09 arises, replace the Processor Board

The "hello" message contains a line identifying the amplifier and the firmware revision number, a line containing the serial number of the amplifier that the Processor Board (actually the microprocessor) was instalied in (or for), a line indicating total amplifier on–time, two lines identifying the heater on–times of each tube, and finally a line indicating the fault status. If the "hello" message is not transferred, continue with the section below named No Response.

If the hello message format appears, press the Enter key or type the serial command "S" several times (Enter is also accepted as the command to return status). The microprocessor should return the string "ready" each time. If this does not occur, continue with the section below titled incorrect Response.

It may be possible to clear a fault (particularly a microprocessor fault) by recycling the circuit breaker off and on a few times. If the indicated faults cannot be corrected by this method, continue with the procedure Fault Isolation.

Section 4.6 Processor Board Diagnostics (Continued)

No Response

This section is relevant to a Processor Board that does not send the “hello” message (see above) at power–on. This message is approximately 50 characters long and should be sent at 9600 baud, no parity, 1 stop bit. Failure to send this message is an indication that:

1) one (or more) of the power supplies is incorrect:
2) the RS–232 link is incorrect;
3) the oscillator is incorrect:
4) the microprocessor is operating in the wrong mode;
5) the microprocessor is in reset;
6) the microprocessor is being interrupted;
7) something is grossly wrong with the microprocessor.

These items are interactive and are difficult to test independently. The order in which they have been listed above is the order in which faults are most probable. Each item is addressed below.

1. There are two probable power supply failures: the + 5 volt (+/– 0.1 volt) supply and the –5 volt (+/– 0.5 volt) supply. If either of these power supplies is out of tolerance, check prior to the bridge rectifier (BR1) for the correct AC voltage of about 10 volts rms. This measurement will determine whether the problem is on the Processor Board or in the AC Switching Module (fuse, cables, transformer, etc.).

2. The RS–232 can be checked with an oscilloscope. After turning main power on, measure voltage at connector J2204, pin2 (TxD from controller); it should be –5 volts DC. Pin 5 (CTS from external monitor) should be –3 volts to –12 volts DC. If these are correct, check for data transfer on TxD at the assigned baud rate (9600 usually, possibly 1200 if the microprocessor BAUD register has been altered; see Section 2.2). If a there is no data, the failure is probably on the Processor Board.

NOTE:
Be sure to check that the external RS–232 terminal is indeed operational before deciding to replace the Processor Board for an RS–232 failure.

3. The microprocessor E–clock (U16, pin 27) should be a 2 Mhz square wave, 50% duty cycle. If not, then either the microprocessor (U16) has failed or the main oscillator (consisting of RB, R9, C16, C19, O1, and X1) is not working. Replace the Processor Board.

4. The microprocessor will operate in 1 of 4 modes depending on the state of MODA (68HC1 1 pin 24) and MODB (pin 25) pins at power–on. These two pins should be +5 volts resulting in the “external address mode”. This mode can be identified after power–on as follows:
   a) U16, pin 27 “E” should be a 2.0 MHz square wave, 50% duty;
   b) pin 26 “AS” should be a 2.0 MHz square wave, 25% duty;
   c) pin 25 “MODA” should be an asynchronous square wave;
   d) pin 24 “MODB” should be +5.00 volts.
   If any of these are incorrect, replace the Processor Board.

Section 4.6 Processor Board Diagnostics (Continued)

5. The 68HC11 /RESET pin 39 should be +5.0 volts DC. If it is fixed at TTL low, then circuitry on the Processor Board is most likely causing a reset. If pin 39 is low–going pulses (pulse width about 2 microseconds occurring every few milliseconds), then the microprocessor itself is causing the problem (watchdog is firing); replace the Processor Board.

6. Microprocessor pin 41 (/IRO) should be +5.0 volts DC. If it is TTL low, then most likely there is a Processor Board problem associated with U13, U11 or U10. The RF MON and PCM lines should be verified to be correctly functional before replacing the Processor Board.

7. If more than one of the above, or perhaps all of the above are occurring, then a good assumption is that the microprocessor has grossly failed. Replace the Processor Board.

Incorrect Response

This section is most relevant if the Processor Board sends the “hello” message correctly, but does not respond to serial commands. This behavior is most likely an indication that:

1) the RS–232 communications is incorrect;
2) the amp failed its selftest;
3) the watchdog (COP) has fired;
4) something is grossly wrong with the microprocessor.

This section is similar to the “No Response” section above, except that the microprocessor appears to be partially functional since the “hello” message was sent. However, no apparently valid faults are indicated, only incorrect functioning.

1. If the “hello” message was received, the microprocessor portion of serial communications (at least output) is functional. Check the baud rate (9600), parity (none), data bits (8), start bits (1 +), and stop bits (1). Connect an oscilloscope to connector J2204 pin 3 (RxD), and attempt to transfer a few characters from the external serial computer. This will verify whether data is reaching the Processor Board correctly. If data transferral is valid, then the RS–232 circuitry on the Processor Board (maybe including the microprocessor) has failed. Replace the Processor Board.

2. The firmware selftest could fail in such a way that DTR (J2204 pin 20) is left false (–5 volts). For proper communications to occur, the microprocessor should be holding DTR high (+ 5 volts). This failure could prevent the terminal from transferring characters. If cycling the circuit breaker does not correct this problem, and the Processor Board is the source of the –5 volts, then replace the board.

Section 4.6 Processor Board Diagnostics (Continued)

3. The COP watchdog system requires firmware to reset the timer before it times out and forces an interrupt. If this does not occur, then the microprocessor and/or firmware is not operating properly. This situation can be identified by looking at the /RESET pin 39 (U16) which will go low for 2 microseconds every time the COP times out. If this is observed after cycling the circuit breaker, the microprocessor has faiied; replace the Processor Board.

Fault Isolation

This section pertains to the most general of problems; that is, the serial communications is working, and a fault is displayed directly related to the Processor Board. Also, this section pertains to a fault code issued for another module, but that module does not seem to be faulty.

The possible problem areas on the Processor Board that could be the source of the-trouble are:

a) Motor control,
b) Amplifier tuning and AFT,
c) FET bias control,
d) Analog fault testing.

Each of these topics forms its own section below. Proceed with the most likely candidate based on the fault code exhibited.

Motor Problems

First confirm that serial communications is working as detailed above.

The bottom motor is #1, counting up, with the top motor being #4. The motors can be independently turned to any location while the amplifier is in OFF mode using the serial “T” command:

T<n> <dest>
where n = 1,2,3, or4 (motor #), and dest = 0 to 65535.

NOTE:
An attempt to command a motor past its maximum will result in hifting the hardware limit (very noisy). This should not damage any of the hardware, but it should be avoided since the shaft couplings might slip leaving the amplifier mistuned.

The maximum physical step count for each motor is defined in Table 2–1, Chapter 2.

CAUTION:
The motor drivers can be damaged due to overheating. In the normal usage of the amplifier, the stepping motors are driven for mode changes and/or AFT only. The motor drivers are not designed to turn the motors for extended periods of time without the side panels in place.

Section 4.6 Processor Board Diagnostics (Continued)

The motors use a washer count ring to find the zero location and limit the number of steps. If the zero sensors fail, then mistuning will result. The motor positions can be sampled by reading the Address Codes (see Chapter 3 commands and codes). Also, permanent address location 7000h can be used to read the zero sensors to verify that the microprocessor is detecting zero. Absolute address 7000h is defined to be:

bit 0 = cover interlock switch 1;,
bit 1 = cover interlock switch 2;
bit 2 = zero sense for MOTOR 1 (high indicates motor at zero);
bit 3 = zero sense for MOTOR 2;
bit 4 = zero sense for MOTOR 3;
bit 5 = zero sense for MOTOR 4;

Confirm that all four motors turn freely while driving their corresponding capacitors using either the serial “T” command or “Z” command. Return the motors to zero with the “Z” command, and confirm that each zero sensor is read correctly.

If all motors fail to turn, the +32 volt supply (from the Power Control Board to the Processor Board) should be examined. If the +32 volt supply on the Processor Board is correct, then the problem is probably on the board; replace it.

If at least 1 motor turns correctly, determine whether a motor assembly or a motor driver (U21 or U22) has failed. Try driving the nonworking motor with a driver from a working motor by connecting the suspect motor harness to a known working connector (P2205–P2208). Be sure to note which connector (P2205–P2208) is the driver when using the “T” command, and return all motor harnesses to their original connectors when finished. Also, try driving a working motor with the suspected driver.

The results of these last tests will determine whether the problem is the motor itself, or is the driver located on the Processor Board (or perhaps a cable problem from a driver to a motor). If one of the motor driver chips has failed, replace the Processor Board.

Amplifier Tuning and AFT

This section pertains to an amplifier that can be brought into STANDBY and switched between HEAD and BODY modes. The attempt to bring it into OPERATE causes the amplifier to be mistuned (bandwidth skewed or forward power insufficient), or displays a tuning related fault code (forward power too high or perhaps high plate currents). This section also assumes that other more likely candidates such as Solid State Amplifier and VTAC problems have been more or less ruled out.

Make certain that AFT is enabled (see Chapter 3), and command the amplifier into STANDBY. There are 2 EEPROM addresses which control the enabling of AFT. B62Bh is the global AFT enable byte where 00 enables AFT, and anything non–zero (normally FFh) disables it. The serial commands “A+” (writes 00) and”A–” (writes FFh) should control AFT. Confirm this by executing “A+” and “A–”. If this does not work (read the EEPROM) then the Processor Board has failed.

Section 4.6 Processor Board Diagnostics (Continued)

Also relevant is EEPROM address B625h which dictates whether or not the PA Phase Detector is to be used for BODY mode tuning. A 00 bit value indicates the detector is enabled, FFh (or anything non–zero) indicates it is disabled. The AFT algorithm depends on whether or not the PA Phase Detector is enabled.

If AFT is enabled, then it will occur whenever the amp is brought from STANDBY to OPERATE, and will occur regardless of a mode change having occurred previously. If the PA Phase Detector is enabled, then the AFT algorithm will be tune IPA, tune PA, tune IPA, tune PA, OPERATE; otherwise AFT will be tune IPA, OPERATE.

Command the amplifier into the desired mode, remove RF input (including UNBLANK), and bring the amp into OPERATE. When the amplifier is in OPERATE, read motor positions 1 and 3 (only MOTOR 1 in HEAD mode). The motor positions are found at in the RAM Address Codes (see Chapter 3).

Execute AFT by commanding the amplifier to STANDBY and then back to OPERATE. Compare the positions of the IPA and PA tuning capacitors (MOTORs 1 and 3) with the positions taken from the first AFT. If these two compare within 10 steps for MOTOR 1, and within 50 steps for MOTOR 3, then AFT is most likely working correctly. Try the procedure a few more times to ensure that AFT is working consistently. If the motors do not turn at all, check the AFT enable, and refer to Motor Problems above.

If the motors are turning, but AFT is not working correctly, it is possible that the Solid State Amplifier oscillator has failed. Perform the Solid State Amplifier diagnostic section to verify correct osciliator function. If the Solid State Amplifier is not the problem, refer to the VTAC diagnostics to check the phase detectors.

If the motors are turning in response to AFT, then the microprocessor is probably not the problem. However, it is possible that an A/D conversion on the Processor Board is not occurring correctly. Refer to Analog Testing below..

FET Bias Control

Perform these diagnostics if the FET bias network on the Solid State Amplifier Board has identified the FET bias network as faulty, and the problem is apparently not on the Solid State Amplifier.

NOTE:

Perform the Solid State Amplifier diagnostics first. Any biasing problem with the FETs is most likely located on the Solid State Amplifier Board.

The only problems in FET biasing which can be caused by the Processor Board are the bias targets, serial SPI problems, one A/D channel, and the 0–20 volt DACs used for fine adjustment on the Solid State Amplifier.

Section 4.6 Processor Board Diagnostics (Continued)

A very useful routine for this section of diagnostics is the “ballpark” routine as discussed in the theory sections of Chapter 2. During normal operation, the bailpark routine is executed as the last step going into STANDBY. It is possible to invoke the ballpark routine with the serial “F” command by using the serial “MW” command to load the “FCMD” EEPROM addresses as follows:

“MWB629 CO” = address of BALLPARK (msb)
“MWB62A 0C” = address of BALLPARK (lsb)
“F” = execute routine.

Each time the “F” command is transferred, the routine will be executed.

The best approach to diagnosing FETs is to use the “F” command to observe the functioning of each of the relevant portions of the biasing system named above.

First confirm the FET bias target currents are correct by reading the RAM Address Codes. It is unlikely that this has failed, but they can be easily verified.

Next observe the FET bias signals (FET1 BIAS – FET4 BIAS) at the outputs of U47–U50 on the Processor Board. The outputs will step from 0–20 volts maximum (20 volts is full range and will probably not be reached during a normal bias algorithm. If there is no output at one of these DACs, replace the Processor Board.

Finally, observe the SPI communications on the MOSI2 line (U27) while issuing an “A” command to address the Solid State Amplifier. This is not a very likely Processor Board problem, or the Front Panel display would also most likely be incorrect. Figure 2–1 and Figure 2–2 in Section 2.2 illustrate the SPI timing.

Analog Testing

This section is intended to provide information for utilizing the Processor Board A/D conversions for general amplifier diagnostics. There really is very little that can actually fail with the Processor Board portion of A/D sampling; the multiplex switches could fail, a connection could become loose or noisy, a resistor could open, or the microprocessor itself could fail. None of these is very likely to occur on a board that has worked in the past. The most likely cause of incorrect A/D samples is the source of the sample.

As mentioned in Chapter 2, thirty–two analog test points within the amplifier are sampled and tested by the microprocessor. A complete listing of the A/D Address Codes, targets of samples, A/D conversion values, and fault limits is provided in Table 2–2. All A/D channels may be read through the SCM or serial interfaces as described in Chapter 3.

Section 4.6 Processor Board Diagnostics (Continued)

One very useful feature of the amplifier is the capability of providing an internally generated RF pulse to update the A/D readings. This feature is known as the “blast mode”. There are four possible versions of the “blast mode” executed with the serial “B” command:

“B1”: head mode to head port output;
“B2”: head mode to 50 ohm dummy load in RF Monitor Module;
“B3”: body mode to body port output;
“B4”: body mode to 50 ohm dummy load in RF Monitor Module.

The “blast modes” utilize the Solid State Amplifier’s on–board 63.86 MHz oscillator which is normally used for AFT. In all four blast modes, the full power of the oscillator will briefly be unblanked, amplified, and routed to the specified output. This is approximately equivalent to a single RF pulse 100 microseconds wide at approximately –13 dBm input put through the system. After this pulse has completed, all of the RAM variables and A/D samples will be updated by the pulse and may be read to provide useful information.

Section 4.7 Power Supply Diagnostics

Amplifier power supply diagnostics may be subdivided into three subsections: the AC Switching Module. the High Voltage Rectifier/Filter Board, and the Power Control Board. Each of these areas is covered separately in the three following Sections.

It will be very helpful to be familiar with the theory of operations description in Section 2.3 of Chapter 2. The A/D sampling of the power supplies by the microprocessor is also an extremely helpful diagnostic tool. Therefore, Chapter 3 material will also be referenced extensively.

Some of the diagnostic procedures require measurements to be made on the amplifier while power is on. See Section 4.1 for a discussion of the cover interlock switches and the procedure for defeating them. Pay particular attention to the cautions noted there.

WARNING:

Lethal voltages and currents exist within this amplifier. Please follow all warnings and cautions noted. Special high voltage test probes are required to directly measure the high voltage supplies. Any such probe should be used extremely carefully. Consult schematics and interconnection diagrams thoroughly to determine the dispersion of high–level voltages. Short all parts to be handled to ground after amplifier main power is turned off; several large capacitors are used in the amplifier.

Section 4.7.1 AC Switching Module Diagnostics

Introduction

The AC Switching Module performs all of the AC line switching and distribution functions required by the amplifier. The module is designed to be easily replaced in the field in case of a failure. Note that dangerous voltages are present within this module and great care must be taken to avoid electrical shocks.

Many power supply voltage problems can be tracked down to fuse failures. Therefore, it is recommended that one start there when trouble shooting power supply problems. Fuse assignments are described in Section 4.3 of this Chapter and on the Ac Switching Module schematic B6–013–2110.

Three–phase line power with a safety ground is required by the amplifier. The rated line to line voltage is 208 volts AC (+/– 10%). All three phase–voltages must be present for proper operation of the amplifier's power supplies. Each phase–voltage may be measured on the screw terminals terminating the line cord wires in the AC Switching Module rear panel circuit breaker. The line to safety ground (green/yellow wire marked with a circled ground symbol) nominal voltage in a 208 volt three–phase balanced system is 120 volts AC.

A neutral power return conductor is not needed for this design since all of the amplifier's loads are line to line. Phase rotation of the three–phase power is also not critical, and is therefore not specified for this amplifier

Fuses

Fuses are used to protect many of the circuits within the amplifier. Section 4.3 describes the fuse locations and functions as well as the ampere ratings to be used. Turn off the amplifier's rear panel circuit breaker to remove dangerous voltages before removing any fuses for inspection and test.

The best method of checking the "slow blow" fuses used in the amplifier is a resistance test using an ordinary ohmmeter. The DC resistance of a good fuse should be less than two ohms. Replace any fuses with DC resistances substantially higher than this. Be sure to replace fuses as marked on the amplifier.

Control Power Section

Transformer T1 provides two voltages which are used to power continuous control circuits in the amplifier. A dual 10 volt–rms secondary winding is used by the Processor Board for +5 volt and –5 volt regulated supplies. A 25 volt rms secondary winding powers the +32 volt supply from which the +24 volt regulated supply is also derived. These windings must always be powered when the amplifier's rear panel circuit breaker is on.

Section 4.7.1 AC Switchinp Module Diagnostics (Continued)

A quick test of the +5 volt supply and circuitry is to observe the Front Panel Display Board indicators. If any LED is lit, at least a partial excitation of the +5 volt supply must be occurring. A quick test of the 25 volt–rms winding is to measure the +32 volt supply voltage.

Fuse F3 and F6 protect the T1 transformer primary winding, and fuses F1 and F2 protect the 10 volt–rms secondary windings. However, the 25 volt–rms winding has an embedded thermal fuse which will permanently open if the transformer winding exceeds an elevated temperature. The 25 volt–rms transformer voltage can be measured on the AC Switching Module's rear panel connector J2101 pins 11 to 12. If there is no AC voltage output from the 25 volt–rms winding, replace the AC Switching Module.

The two 10 volt–rms winding voltages can be measured at J2102 pin 3 to 2 and 3 to 4. If these voltages are not correct, check the fuses. If the fuses are not high impedance and the 25 volt–rms output is correct, replace the AC Switching Module.

Low Voltage Power Switching

The low voltage power switching is done with relays K1 and K2. Relay K1 applies power to the two front panel fans through fuses F7 and F8, to the tube cooling Blower Assembly through fuses F4 and F5, and soft starts the +100 volt power supply through fuses F10, F11 and F12.

The +100 volt supply soft–start is accomplished by using 300 ohm resistors to limit the inrush current in two of the three Low Voltage Transformer primary phases. Power switching relay K2 bypasses the current limiting resistors after the filter capacitors receive their initial charge. The soft–start is performed while there is no load on the supply.

A fault 50 or 51 indicates an unsuccessful soft–start sequence. This could result from a missing phase due to relay K1 failure, open fuses F10, F11 or F12, open connector J2101, J2001, or J2402, shorted or open rectifier diode on the Power Control Board (D26 through D31), or a load on the +100 volt supply. The two primary loads on the +100 volt supply (the +48 volt supply regulator and the PA tube heater regulator) should not be enabled by the microprocessor during this time.

Check all fuses for high impedance and replace as needed. See Section 4.7.3 for a detailed diagnostic description of the +100 volt supply.

High Voltage Power Switching

The high voltage power switching is done with relays K3 and K4. Both the +3KV and +6KV supplies are powered from the same three phase rectifier 4.5KV HV Transformer. The soft–start of these supplies is accomplished by using 100 Ohm resistors to limit the inrush current in two of the three transformer primary phases. Power relay K4 (or solid state switches SW1 and SW2 in AC Switching Module 2) bypasses the current limiting resistors after the filter capacitors receive their initial charge. Refer to Section 4.7.2 for diagnostics of the high voltage power supplies.

Section 4,7.1 AC Switching Module Diagnostics (Continued)

Circuit Breaker Trips

The circuit breaker in the AC Switching Module is used to protect the amplifier wiring and the 4.5KVA HV Transformer against failures not protected by the arc detect and overload circuitry. The circuit breaker is also used as the line disconnect switch.

The breaker should never trip for an overload on a non–high voltage power supply. The protective fuses will always open before the breaker trips (if they are the proper size).

The most probable causes of a circuit breaker trip are a shorted 4.5KVA HV Transformer primary or secondary winding, a high voltage short while in STANDBY or OPERATE, a high voltage arc with a faulty arc detector circuit, welded K4 relay contacts in AC Switching Module (not possible in AC Switching Module 2), and excessive duty cycle of high power RF pulses.

Section 4.7.2 High Voltage Power Supply Diagnostics

Introduction

The +3 KV and +6 KV high voltage power supplies are located in the bottom High Voltage Cavity. The three–phase 4.5 KVA HV Transformer connects directly to the High Voltage Rectifier/Filter Board. The AC Switching Module provides control of the 208 volt three–phase line power required by the transformer primaries. Both of the +3 KV and +6 KV supplies are controlled simultaneously by relays K3 and K4 (K4 is replaced by solid state switches SW1 and SW2 in AC Switching Module 2) in the AC Switching Module.

WARNING:

Dangerous voltages are generated within the high voltage power supply circuitry. THESE VOLTAGES CAN KILL! Special high voltage test probes are required to measure these voltages directly. Only use equipment rated to above 10 KV on these circuits. Before accessing the high voltage circuitry, wait at least three minutes after turning off the amplifier’s rear panel circuit breaker. Always discharge the +3 KV and +6 KV positive supply terminals with a grounding strap before working with the high voltage circuitry.

High Voltage Supply Starting Problems

Both the +3 KV and +6 KV supplies are sort–started at the same time. The soft–start limits the inrush currents into the transformer and subsequently through the rectifiers into the filter capacitors. The capacitor filters store hundreds of Joules of energy and take a substantial time to fully charge up. Multiple microprocessor tests are made on the supply voltage during the charging process. A supply component or load problem reducing the voltage on one supply may be reflected as a low voltage on the other supply; this can make it hard to distinguish the origin of a problem.

Section 4.7.2 High Voltage Power Supply Diagnostics (Continued)

Possible sources of a high voltage supply soft start problem are:

1) missing phase–voltage on the transformer primary;
2) shorted winding in the transformer;
3) shorted or open high voltage rectifier diode;
4) load on a supply.

Each of these problems are diagnosed as discussed below.

1. A missing phase–voltage is most likely traceable to the AC Switching Module or connectors. First, check the AC line power on the circuit breaker in the AC Switching Module on both sets of terminals (with breaker on). Secondly, check the resistors R1 and R2 in the AC Switching Module. Finally, observe the soft–start voltages being enabled as going into STANDBY at the AC Switching Module output connectors J2101 and J2006. These steps should verify the existence of the three phase–voltages.

2. The 4.5KVA HV Transformer primary and secondary windings may be checked for opens or shorts with an ohmmeter. Turn the circuit breaker off and measure the primary winding resistances at the J2006 connector and the secondary winding resistances at the “W” terminals on the HV Rectifier/Filter Board.
3. Use a diode checker to verify the operation of diodes D13 through D24 on the HV Rectifier/Filter Board.
4. A soft–start load can be discovered by disconnecting +3 KV and +6 KV cables (one at a time) from the HV Rectifier/Filter Board and restarting the amplifier. If the soft–start fault goes away, the most likely sources of the problem are the tube bias circuitry, the 7.5 KV ceramic capacitors, and the vacuum tube.

High Voltage Run Problems

High voltage problems at the run stage are a little different from soft–start problems in that the system has been running at proper voltage during the–soft start sequence. High voltage run problems may be broken down into two classes: unacceptable voltage faults, and arc related faults. Each of these is discussed below.

1. Unacceptable voltage faults most likely represent a low voltage condition. The first step is to check for low, high, or varying line voltage during STANDBY and during high power operation.

   Another cause of these faults is unusually long and frequent UNBLANK commands. This may be checked at the PCM port.

   The other most probable cause of this condition is due to the tube bias circuitry or the tube itself. Check tube cathode bias levels on the Power Control Board (Section 4.7.3), and check for tube failure by reading the RAM Address Codes associated with plate and grid currents during OPERATE. High values (beyond target values) are a sign of a failing tube.

Section 4.7.2 High Voltage Supply Diagnostics (Continued)

2. Arc related faults indicate that an extremely high load current on either the +3 KV or +6 KV power supply has occurred. Such currents are usually due to an arc condition either within a vacuum tube, across an air gap or inside a high voltage component. Tube arcs usually (but not always) burn off sharp points within the tube and subside quickly. An arc inside a tube usually cannot be heard; whereas, external arcs (in the air) usually sound like a sharp crack.

   Surface contamination on high voltage parts caused by finger prints or dust can establish an arc path. Cleaning these surfaces will reduce the possibility of ion tracking of the surface which results in a lower voltage breakdown potential.

   High voltage component failures are not always detectable by visual inspection. Internal breakdowns may not leave evidence on the outside surface. The break–down may also only occur at elevated voltages making ohmmeter testing only effective for severe failures.

   Visual inspection and component isolation are the two recommended diagnostic techniques for finding high voltage breakdowns. The fault code defines which tube stage to investigate. Look for arc tracks, cracked components and smoke deposits to pinpoint defective component location. Progressively disconnecting the tube and its high voltage circuitry and restarting the amplifier can be used to isolate the faulty component.

Section 4.7.3 Power Control Board Diagnostics

Introduction

The Power Control Board contains many complex and interactive circuits. It is designed to be a field replacement module requiring no field adjustments. Always check the fuses in the AC Switching Module relevant to the power supply circuitry on the Power Control Board as the first step in diagnosing power supply problems. Also note that often a low power supply voltage is not be due to a faulty supply but an abnormal load condition.

Diagnosing problems in the Power Control Board may be complicated by the protective actions of the microprocessor. Invalid voltages and over current conditions will generate a fault condition and a power supply shutdown. A trial Power Control Board substitution can often be the most effective trouble shooting technique for some failures.

Power Control Board Diagnostics (Continued)

+32 Volt Supply

The +32 volt supply should be powered continuously if AC power is being supplied to the amplifier with the rear panel circuit breaker on. The transformer and fusing are located in the AC Switching Module. A convenient test point to measure the +32 volt supply voltage is on the Power Control Board wire through FB12 near connector P2402.

If +32 volts is missing look at the fuses F3, F6 and F9. Then check connector J2101 for the 25 volt–rms (nominal) output from the AC Switching Module). If the AC voltage is present, then either the bridge rectifier BR1 is bad, or a load is pulling the supply down. If possible try replacing the Power Control Board, or try removing the loads from the supply (see Table 2–3, Chapter 2).

+24 Volt Regulated Supply

The +24 volt supply is powered from the +32 volt supply, and is active whenever the circuit breaker is on. The +24 volt supply is of a complex design incorporating foldback current limiting for protection. The circuit has been adjusted at the factory utilizing calibrated loads to set the current limit point. These adjustments should not need to be made in the field. The current limit circuitry, if misadjusted, can disable the voltage regulator.

If the +24 volt supply is low (test point TP7), first check for proper +32 volt supply voltage at FB12 and for + 12 volts at the anode of D33. The supply's load current may be deduced by measuring the voltage across R98. The supply is in current limit if pin 6 of U9 is below 5 volts. If current limit or very high current exists, attempt to isolate the load (see Table 2–3, Chapter 2).

The microprocessor also can shutdown the regulator through "FLT 3". Check to see if pin 2 of U10 is above 0.4 volts. If it is, try putting pin 2 to ground temporarily to see if the regulator begins working. If it does (including no current limit), the Processor Board is at fault.

Also check the regulator's reference voltage at pin 6 of U10. This voltage should be between 6.8 to 7.5. If not, replace the Power Control Board. If the +24 volt supply is high, check Q27 for shorted emittier to collector and R92 for an open wiper (adjustment should adjust voltage). Replace the Power Control Board.

+100 Volt Supply

The +100 Volt supply is an unregulated supply operating around 100 volts nominally. Three–phase power to its transformer comes from the AC Switching Module. The supply is soft–started through 300 Ohm resistors in two of its three primary lines when power switching relay K1 closes. This limits the inrush current to the transformer, rectifier diodes and filter capacitors on the Power Control Module.

Section 4.7.3 Power Control Board Diagnostics (Continued)

The soft–start occurs at the same time as AC power is switched to the fans and blower (immediately as commanded into STANDBY). The soft–start sequence terminates approximately one second later when power relay K2 bypasses the current limiting resistors. If the fan and blowers don't turn on with a "go to standby" command, the problem is either the Processor Board or the AC Switching Module

+100 Volt Supply Start Problems

The most probable sources of a +100 volt supply soft–start problem are:

1) missing phase to the Low Voltage Transformer primary,
2) shorted or open winding in the Low Voltage Transformer,
3) shorted or open rectifier diode,
4) load on the supply.

Each of these items is diagnosed as discussed below.

1. A missing phase–voltage is most likely due to a problem in the AC Switching Module or in the transformer itself. First, check AC line power in the AC Switching Module both before and after the circuit breaker. Also check the resistors R3 and R4. Finally, look at the output connector J2101 to observe the soft–start voltage output.

2. Check the Low Voltage Transformer primary and secondary winding resistances at connector J2001 for shorts or opens.

3. Use a diode checker to verify the function of diodes D26 through D31 on the Power Control Board.

4. Check the +48 volt supply and the PA tube heater supply for activity during the soft–start sequence. These supplies should not be enabled until after the soft–start sequence.

+100 Volt Supply Run Problems

An unacceptable +100 volt supply voltage during normal amplifier operation would be due to lack of input power, a defective component in the +100 volt supply circuitry, or an excessive load on the supply. All of the diagnostic steps covered above for the soft– start problems apply.

+48 Volt Regulated Supply

The +48 volt supply is a single ended switching–type powered from the +100 volt supply. Current limiting circuitry is built in which will limit the output current to slightly over 2.5 Amps to protect the supply during fault conditions. This supply is used only for the high power RF FET stages on the Solid State Amplifier Board.

Section 4.7.3 Power Control Board (Continued)

CAUTION:

High voltages and large quantities of stored energy (external 50,000 microfarad capacitor) require cautious actions when working with the +48 volt supply circuitry. The power switching FET used can be destroyed by excessive gate to source voltages. Be very careful with scope and voltmeter probes.

If the +48 volt supply regulator output voltage is greater than 50 volts (test point TP1) after the +100 volt supply soft start, the failure is on the Power Control Board; replace it.

If the +48 volt supply regulator output voltage is lower than 45 volts after the +100 volt supply soft–start, check Q2 source lead for the presence of +100 volts. If not, replace the Power Control Board.

Check to see if the regulator is in current limit by looking at the voltage drop across R1 and for a voltage greater than 0.4 volts at pin 1 of U1. If the supply shows high current, attempt to isolate the load (probably Solid State Amplifier FETs).

The +48 volt supply regulator is controlled by the microprocessor, if pin 4 of U1 is – greater than 0.5 volts, check the /ENABLE line for a valid low logic. If not, the problem may be on the Processor Board.

If any of the below items are invalid, replace the Power Control Board:

a) pin 14 of U1 reference voltage between 4.75 and 5.25 volts;
b) pulse width ramp signal on pin 5 of U1 is 50 to 60 Khz, 0 to 3 V sawtooth;
c) pin 9 of U1 drive current pulse (0 to about 10 volts;
d) pin 9 of U1 drive current present but O2 drain static.

PA Heater Regulated Supply

The PA tube heater regulator is a floating push–puli transformer–coupled design powered from the +100 volt supply. This isolation is required because the PA tube's cathode is internally connected to its heater. Measurements on the PA tube heater supply output circuitry past T1 must not be made referenced to ground because of complications from the PA tube"s bias circuitry. The loaded (tube heater on) output voltage is factory set to 15.2 volts to compensate for wiring losses.

CAUTION:

High voltages and large quantities of stored energy require cautious actions when working with this circuitry. The power switching FETs may be destroyed by excessive gate to source voltages. Be very careful with scope and voltmeter probes.

Section 4.7.3 Power Control Board Diagnostics (Continued)

The PA tube heater supply regulator is normally enabled about one second after the amplifier receives the “go to standby” command. The PA tube heater itself has a very low resistance when it is cold, and the regulator will initially start in current limit of about 18 Amps. The output voltage will gradually climb to 15.2 volts over a period of about 10 seconds as the heater warms up. The supply output current will then stabilize at about 15 amps.

The output current can be estimated by measuring the voltage on pin 16 of U2 and multiplying by 10 for amps (1.5 volts = 15 amps).

PA Heater Supply Starting Problems

The PA tube heater current is measured during the start phase when the heater is cold. If the start current is low check to the the cold tube heater for a resistance on the order of 0.15 ohm at both connector J2404 and the terminals above the Blower Assembly labeled PA HTR +/–.

If the start current is high, replace the Power Control Board.

PA Heater Supply Run Problems

The PA tube heater supply current limits may be used to detect PA tube heater failures. The lower limit is about 12 amps, and the upper limit is around 16 amps. The typical heater failure will drop its current to about 60% of normal (8 to 9 Amps) because one of the two heater wires opens up.

Diagnosing a genuine tube heater failure and a PA tube heater supply failure may be done as discussed below. The currents indicated in the discussion are calculated from the voltage on pin 16 of U2 as noted above.

If the current is less than 12 Amps and the output voltage measured across test points TP3 and TP2 is about 15 volts, then most likely the tube heater is bad or the wiring is bad. Measure the resistance of the tube heater at the terminals above the Blower Assembly and the resistance of the heater and heater wiring at connector J2404. If the resistance measurements are about one ohm or less, replace the Power Control Board.

If the current is less than 12 amps and the output voltage is also low (less than 15 volts), replace the Power Control Board.

If the current is greater than 16 Amps at about 15 volts output, check for a cable harness short. If the impedance is greater than 0.15 ohms, replace the Power Control Board.

If the current is greater than 16 Amps and the output voltage is greater than 15 volts, the replace the Power Control Board.

Section 4.7.3 Power Control Board Diagnostics (Continued)

IPA Heater Regulated Supply

The IPA tube heater supply is of a linear design powered from the +32 volt supply. The regulator is controlled from the microprocessor, and is enabled at the same time as the PA tube heater supply and the +48 volt supply. The IPA tube heater itself is an isolated load and presents a relatively constant load resistance after warm up. Therefore the regulator is not required to operate over a wide dynamic range. Most of the tube heater current is provided through two fixed resistors, R106 and 107. A variable current is supplied through R105 and regulator VR2. This design automatically limits the inrush current to a cold tube heater. The IPA tube heater supply current can be measured by the voltage drop across R47 which is in the return current path from the tube heater.One volt represents one amp of current.

IPA Heater Supply Start and Run Problems

The microprocessor checks for gross heater current errors one second after receiving the “go to standby” command. After 15 seconds the tube currents are more closely watched, and faults are reported as run problems (fault 14). The diagnostic procedures below apply to any IPA heater fault.

If the current is less than 1 amp and the output voltage at test point TP4 is greater than 15 volts, check the IPA tube heater wiring across TP4 and R48 for resistances greater than 8 ohms. If the resistance is lower, replace the Power Control Board.

If the current is less than 1 amp and the output voltage is under 15 volts, then the regulator circuit has failed; replace the Power Control Board.

If the current is greater than 2 amps and output voltage is less than 15 volts, then check for a cable harness wiring short at connector J2404. If the resistance is greater than one ohm, replace the Power Control Board.

If the current is too high and the output voltage is greater than 15, the the regulator has failed; replace the Power Control Board.

Tube Bias circuitry

The tube bias circuitry controls the operating and cutoff cathode to grid bias voltages for both the IPA and PA vacuum tubes. The operating bias levels are dependent upon the anode voltage and vary from tube to tube. Cutoff bias is required while the amplifier is blanked. Idle current bias is applied to the tube only at the beginning of the UNBLANK period except for the initial bias level set by the microprocessor.

The circuitry utilized by the IPA tube is duplicated with only a few minor variations for the PA tube. The following diagnostics directly relates to the PA circuitry, but notes where the IPA circuitry may deviate in procedure.

Section 4.7.3 Power Control Board Diagnostics (Continued)

The +3 KV and +6 KV high voltage power supplies can experience problems in their soft start sequence if the proper tube cutoff bias is not present on the tubes. The lack of cutoff bias problem may reside in a number of places; the following tests will help identify its location.

Check the PA tube cathode voltage at TP6 (IPA tube voltage at TP5) for greater than 100 volts during STANDBY wait (IPA at 32 volts). A low voltage on this line will allow the vacuum tube to conduct current during the high voltage soft–start sequence and result in a fault. The source of this problem can reside on the Power Control Module or with external circuitry (VTAC, HV Rectifier/Filter Board).

Check the TP6 voltage about one second after commanding the amplifier to STANDBY on with connector J2404 disconnected. It should raise up to 100 volts before a tube heater fault returns the system to off (IPA TP5 voltage should be at 32 volts). If the voltage is low, then the problem is probably on the Power Control Board. If the voltage properly returns, then the investigation moves to the external circuitry.

Check the High Voltage Rectifier/Filter Board diodes D1 and D12, the IPA Input Board diode D1, and the PA Input Board diode D1 (isolate the cable harness by unplugging connector J2701, and use an ohmmeter measurement to ground to detect a shorted diode in the VTAC). Also, check the IPA cathode wiring, the PA cathode and heater wiring for ground faults.

The/PA GATE and/IPA GATE signal lines should be at +5 volts. This signal comes from the Processor Board.

PA and IPA idle Current Problems

The range of the PA cathode bias generator is +20 to +50 volts and the IPA cathode bias generator range is +1 to +21 volts. The PA cathode is pulled down from its +100 volt cutoff bias voltage to this bias generator level for periods of less than 20 milliseconds (UNBLANK). The IPA cathode is pulled down from its cutoff bias voltage of +32 volts to its bias generator level during UNBLANK. A digital storage oscilloscope will prove useful in observing these bias transitions.

The Processor Board has two DACs used to set the idle current bias voltages. Buffer amplifiers on the Power Control Board convert these control voltages into rigid bias voltages for the tube cathodes during UNBLANK. DAC output voltage spans are 0 to +20 volts.

The IPA bias voltage on Q21’s drain lead should directly reflect its “IPA BIAS REF” DAC control voltage. In STANDBY, this voltage should be +20 volts. The PA bias voltage as measured on Q23’s drain lead should span the +20 to +50 volt range and reside at +50 volts during STANDBY which is due to a”PA BIAS REF” DAC control voltage of +20 volts.

Section 4.7.3 Power Control Board Diagnostics (Continued)

Observe the drain voltage of Q23 during STANDBY. If it is not close to +50 volts with the PA BIAS REF voltage at +20 volts, replace the Power Control Board. The same observation holds for the IPA bias generator if Q21's drain voltage is not close to the +20 volt IPA BIAS REF.

If the DAC voltages (PA and IPA BIAS REF voltages) themselves are not close to the full +20 volts in STANDBY, look for problems with the DAC circuitry on the Processor Board.

APPENDIX A INTERFACE PORT PIN ASSIGNMENTS

The two center interfacing ports on the rear of the amplifier labeled “RF MON P2202” and”PCM P2203” are subminiature D–type, 9–pin, male connections. These ports must always be properly connected for the amplifier to operate. The D–type, 37–pin, male “SCM P2201” connector must also always be terminated properly. The SCM port has been designed to comply with both of General Electric’s BISYCL and BICYCLE links. Connection to the “SERIAL PORT P2204” connector is optional. Detailed information about SCM and serial commands is provided in Chapter 3.

The interface ports use high–true logic, where logic true is defined to be signal–P greater than signal–N by at least 1.5 volts. False is defined as signal–P less than signal–N by at least 1.5 volts.

NOTE:

An asterisk (*) following the signal name indicates an inverted line polarity (negative logic).

Table A–1 RF MON Pin Definitions

SIGNAL NAME	CONNECTOR PIN #	SIGNAL NAME	CONNECTOR PIN #
UNBLK*–P	1	UNBLK*–N	6
RFLCK–P	2	RFLCK–N	7
HI VOLT REL EN*	3	SPARE	8
RFLCK*–P	4	RFLCK*–N	9
HI VOLT REL +12V	5		

NOTE:

“HI VOLT REL EN” pins 5 and 3 are used to control the +12V (160mA) safety relay mounted on the Processor Board.

Table A–2 PCM Pin Definitions

SIGNAL NAME	CONNECTOR PIN #	SIGNAL NAME	CONNECTOR PIN #
UNBLK*–P	1	UNBLK*–N	6
SPARE	2	SPARE	7
SPARE	3	SPARE	8
SPARE	4	SPARE	9
SPARE	5		

Appendix A Interface Port Pin Assignments (Continued)

Table A–3 SCM Pin Definitions for BICYCLE Link

LINK A		LINK B	
SIGNAL NAME	**CONNECTOR PIN #**	**SIGNAL NAME**	**CONNECTOR PIN #**
DAT0–P	1	DAT0–P	1
DAT0–N	20	DAT0–N	20
DAT1–P	2	DAT1–P	2
DAT1–P	21	DAT1–N	21
DAT2–P	3	DAT2–P	3
DAT2–N	22	DAT2–N	22
DAT3–P	4	DAT3–P	4
DAT3–N	23	DAT3–N	23
DAT4–P	5	DAT4–P	5
DAT4–N	24	DAT4–N	24
DAT5–P	6	DAT5–P	6
DAT5–N	25	DAT5–N	25
DAT6–P	7	DAT6–P	7
DAT6–N	26	DAT6–N	26
DAT7–P	8	DAT7–P	8
DAT7–N	27	DAT7–N	27
ADR0–P	9	ADR0–P	9
ADR0–N	28	ADR0–N	28
ADR1–P	10	ADR1–P	10
ADR1–N	29	ADR1–N	29
ADR2–P	11	ADR2–P	11
ADR2–N	30	ADR2–N	30
ADR3–P	12	ADR3–P	12
ADR3–N	31	ADR3–N	31
STRB3*–P	13	ADR5–P	13
STRB3*–N	32	ADR5–N	32
STRB1*–P	14	STRB1*–P	14
STRB1*–N	33	STRB1*–N	33
STRB2*–P	15	ADR4–P	15
STRB2*–N	34	ADR4–N	34
READ*–P	16	READ*–P	16
READ*–N	35	READ*–N	35
ACK*–P	17	ACK*–P	17
ACK*–N	36	ACK—N	36
STRB0*–P	18	STRB0*–P	18
STRB0*–N	37	STRB0*–N	37
LOGIC GND	19	LOGIC GND	19

Appendix A Interface Port Pin Assignments (Continued)

Table A–4 SCM Pin Definitions for BISYCL Link

SIGNAL NAME	CONNECTOR PIN #	SIGNAL NAME	CONNECTOR PIN #
DAT0–P	1	DAT0–N	20
DAT1–P	2	DAT1–N	21
DAT2–P	3	DAT2–N	22
DAT3–P	4	DAT3–N	23
DAT4–P	5	DAT4–N	24
DAT5–P	6	DAT5–N	25
DAT6–P	7	DAT6–N	26
DAT7–P	8	DAT7–N	27
ADR0–P	9	ADR0–N	28
ADR1–P	10	ADR1–N	29
ADR2–P	11	ADR2–N	30
ADR3–P	12	ADR3–N	31
SPARE	13	SPARE	32
SPARE	14	SPARE	33
ADR4–P	15	ADR4–N	34
READ*–P	16	READ*–N	35
ACK*–P	17	ACK*–N	36
STB*–P	18	STB*–N	37
GND	19		

Table A–5 SERIAL PORT Pin Definitions

PIN #	SIGNAL	FUNCTION
1,7	GND	Ground
2	TxD	Transmit data
3	RxD	Receive data
4	RTS	Ready to send
5	CTS	Clear to send
6	–	Unused
8	CD	Carrier detect
9–19	–	Unused
20	DTR	Data terminal ready
21–25	–	Unused

NOTE:

This amplifier is configured as a DTE (data terminal equipment) device. The amplifier always keeps DTR high (ready to receive data); CTS must be set high by the external RS–232 device for data to be transmitted from the amplifier.