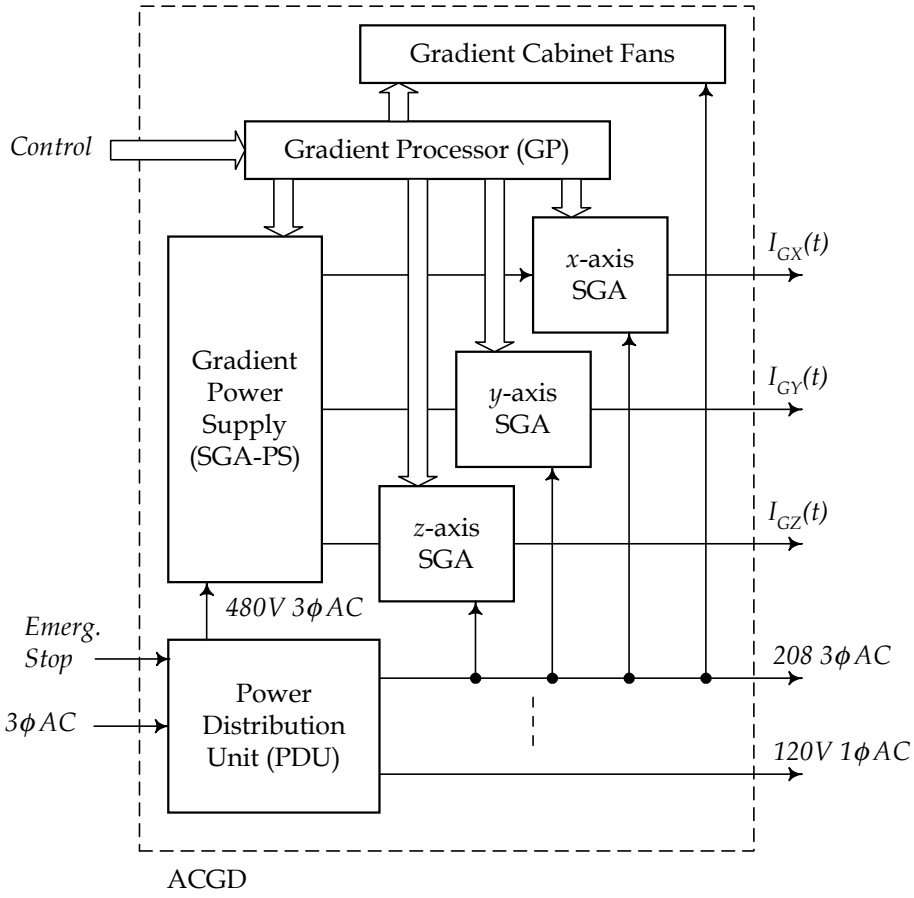
TABLE OF CONTENTS

1- OVERVIEW

The Advanced Control Gradient Driver (ACGD) is a gradient amplifier subsystem for use in the Signa MR/*i* system. It contains a Gradient Processor (the GP), three Switching Gradient Amplifiers (SGAs), a power supply for the SGA's (the SGA-PS), and, and Power Distribution Unit for the system (the PDU). A block diagram for the ACGD/PDU subsystem is shown in Illustration 1-1.



ACGD/PDU CABINET BLOCK DIAGRAM
ILLUSTRATION 1-1

The ACGD/PDU is compatible with line voltages of 200, 208, 380, 415, and 480 VAC, and line frequencies of 47/63Hz. Further information on the PDU can be found in *Direction 2251117, Phoenix PDU Module in 1.0/1.5T Power Cabinet Manual*.

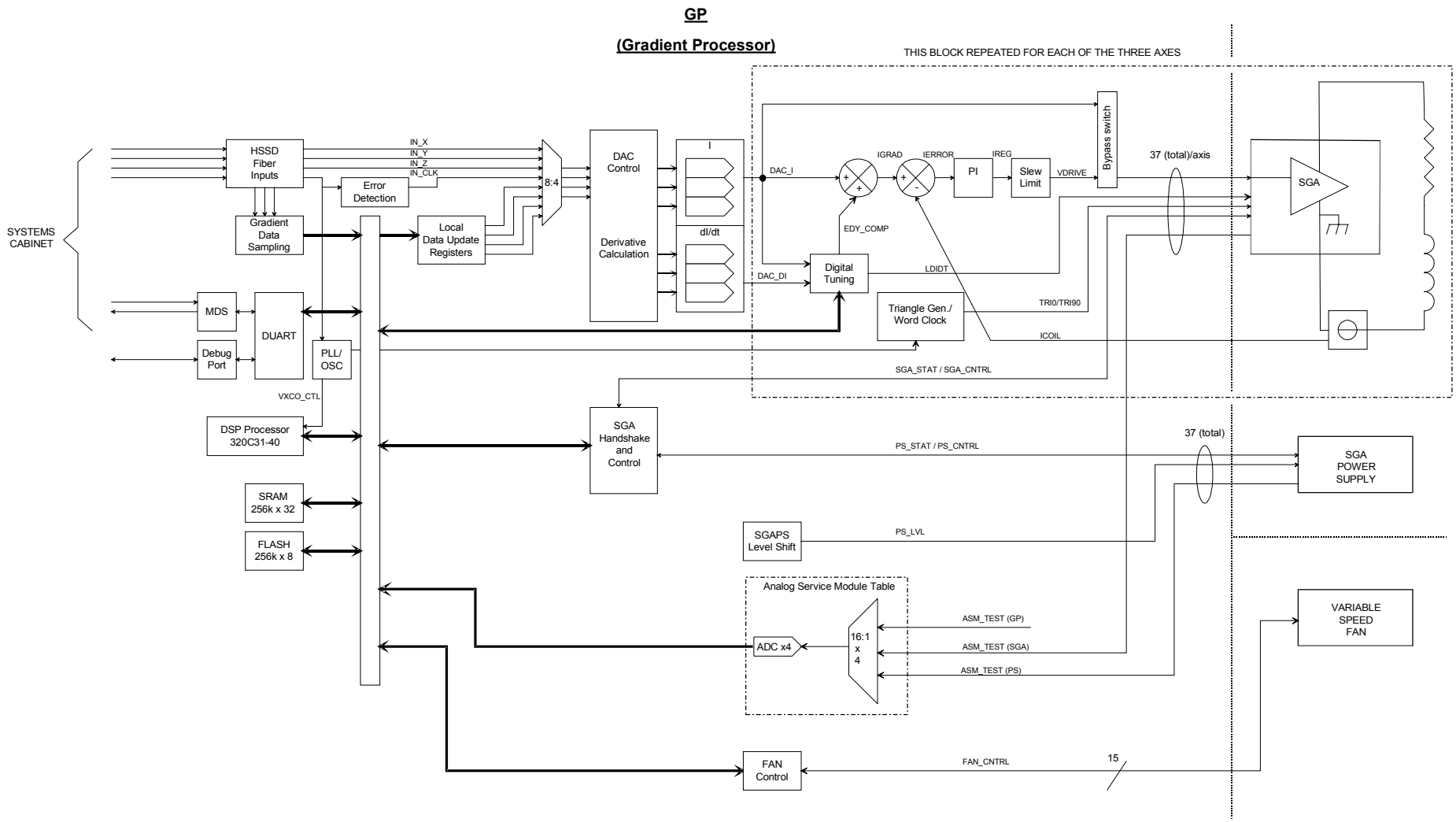
2- GRADIENT PROCESSOR (GP)

2-1 Description

The Gradient Processor (GP) module is an intelligent interface between the LX Systems Cabinet, and the Advanced Control Gradient Driver (ACGD).

All ACGD hardware shall be controlled from the GP. The Systems Cabinet (or suitable test equipment) is required to command the system to ready and report errors. Handshaking between power electronics modules will be done in hardware on the GP to ensure that all power hardware is disabled if a fault occurs. The GP will provide an analog drive signal for the Switching Gradient Amplifiers (SGAs) as well as a power supply level input to the SGA Power Supply (SGA PS). The GP also samples various analog signals on the power electronics modules, and presents them to the system for fault detection and analysis.

Gradient amplifier data is transmitted from the TYME II to the GP over 4 high-speed fiber optic cables. Three of these cables carry 21 bit serial data (X, Y, and Z), the fourth carries a gated 10 MHz clock (CLK). New gradient data is shifted out once every 4 μsec. For each data burst, the GP shall capture the serial data stream and check for framing errors. That data will then be shifted out to the GP DACs on the next 21 bit data burst. In parallel with the gradient data updates, the GP processor shall monitor the status of the SGAs and respond appropriately. Fault conditions shall be handled locally or communicated to IPG via the MDS link.


GP
(Gradient Processor)
THIS BLOCK REPEATED FOR EACH OF THE THREE AXES
SYSTEMS CABINET
HSSD Fiber Inputs
IN_X
IN_Y
IN_Z
IN_CLK
Error Detection
Gradient Data Sampling
Local Data Update Registers
8:4
DAC Control
Derivative Calculation
I
dI/dt
DAC_I
IGRAD
IERROR
IREG
PI
Slew Limit
VDRIVE
Bypass switch
37 (total)/axis
SGA
EDY_COMP
DAC_DI
Digital Tuning
LDIDT
Triangle Gen./ Word Clock
TRI0/TRI90
ICOIL
SGA_STAT / SGA_CNTRL
MDS
DUART
Debug Port
PLL/ OSC
VXCO_CTL
DSP Processor 320C31-40
SRAM 256k x 32
FLASH 256k x 8
SGA Handshake and Control
PS_STAT / PS_CNTRL
37 (total)
SGA POWER SUPPLY
SGAPS Level Shift
PS_LVL
Analog Service Module Table
ADC x4
16:1 x 4
ASM_TEST (GP)
ASM_TEST (SGA)
ASM_TEST (PS)
VARIABLE SPEED FAN
FAN Control
FAN_CNTRL
15

2-2 Mechanical Requirements

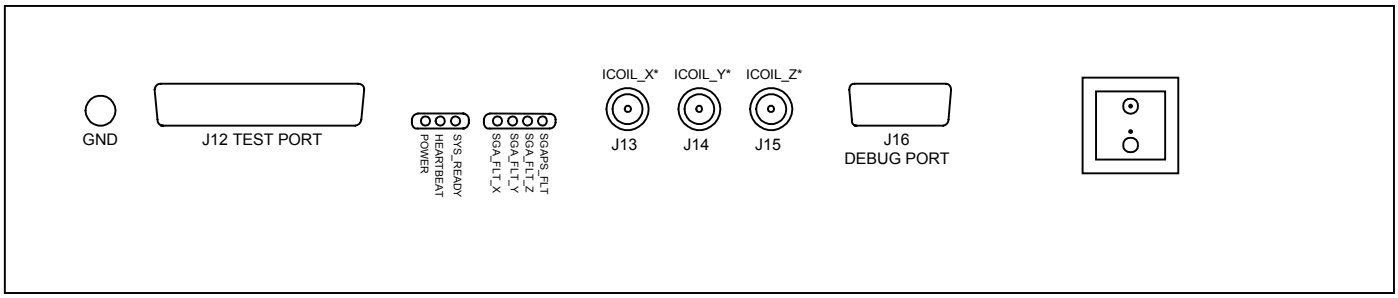
2-2-1 GP Chassis

The GP chassis encloses the GP circuit board assembly and the GP power supply. It resides in the ACGD cabinet. The GP circuit board requires minimal cooling and airflow (≤ 10CFM).

2-2-2 Front Panel Design

The front panel of the GP chassis shall accommodate the connectors listed in the table below, a power switch for the GP circuit board, and all LED's indicated in section 4.3.2.3. See Illustration 2-1 for front panel view.

Connector	NAME	DESCRIPTION
	GND	Grounding stud for scope ground clips
J12	TEST PORT	Connector for 3rd party diagnostics
J13	ICOIL_X	X Current Monitor BNC Connector
J14	ICOIL_Y	Y Current Monitor BNC Connector
J15	ICOIL_Z	Z Current Monitor BNC Connector
J16	DEBUG PORT	Connector for debug terminal use

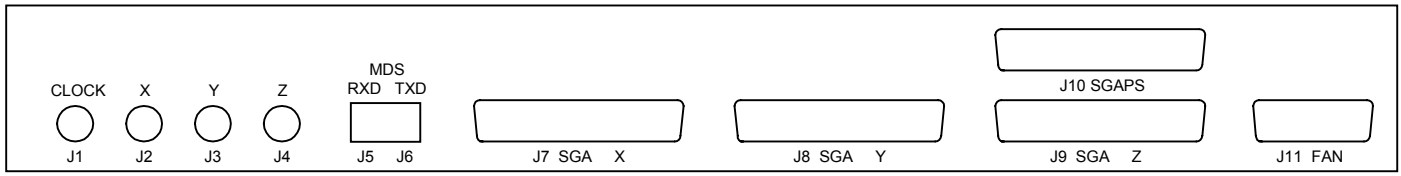


CHASSIS FRONT PANEL VIEW
ILLUSTRATION 2-1

2-2-3 REAR Panel Design

The rear panel of the GP chassis shall accommodate the connectors listed in the table below. See Illustration 2-2 for rear panel view.

Connector	NAME	DESCRIPTION
J1	CLOCK	10 MHz Clock Fiber Optic Connector
J2	X	X Gradient Waveform Data Fiber Optic Connector
J3	Y	Y Gradient Waveform Data Fiber Optic Connector
J4	Z	Z Gradient Data Waveform Fiber Optic Connector
J5	RXD	MDS Receive Connector
J6	TXD	MDS Transmit Connector
J7	SGA X	X SGA Module Connector
J8	SGA Y	Y SGA Module Connector
J9	SGA Z	Z SGA Module Connector
J10	SGAPS	SGA Power Supply Module Connector
J11	FAN	Variable Fan Control Connector



CHASSIS REAR PANEL VIEW
ILLUSTRATION 2-2

2-3 GP Circuit Board

The GP circuit board is 10 layers and 16" x 16". Signal layers are impedance-controlled. Surface mount technology is used primarily. Thru-hole devices are used where no suitable surface mount device is available. Assembly is topside only.

2-3-1 ANALOG design

The GP PWB layout shall receive special attention in the area of analog circuit power and ground, to prevent axis-axis and digital-analog coupling.

2-3-2 Circuit Board LEDs

LED	NAME	COLOR	DESCRIPTION
DS1	POWER	Green	Indicates +5V is present on GP
DS2	HEARTBEAT	Green	Flashing LED indicates DSP operation. Flash sequence indicates which test failed when power-up tests fail.
DS3	SYS_READY	Green	Indicates that entire gradient subsystem is ready to operate.
DS4	SGA_FLT_X	Yellow	On indicates fault on X-SGA module.
DS5	SGA_FLT_Y	Yellow	On indicates fault on Y-SGA module.
DS6	SGA_FLT_Z	Yellow	On indicates fault on Z-SGA module.
DS7	SGAPS_FLT	Yellow	On indicates fault on SGAPS module.

2-3-3 Circuit Board Switches

SWITCH #	NAME	TYPE	DESCRIPTION
S1	RESET	Push-button	Provides manual reset of entire board

2-3-4 Circuit Board JUMPERS

JUMPER #	NAME	POSITION	DESCRIPTION
JP1	IREG_OFFSET_Z	OUT	Changes Z current regulator from integrator to straight gain.
JP2	Z_COMP_OUT	IN	Used with JP3 to set compensation personality.
JP3	Z_COMP_IN	OUT	Used with JP2 to set compensation personality.
JP4	IREG_OFFSET_Y	OUT	Changes Y current regulator from integrator to straight gain.
JP5	Y_COMP_OUT	IN	Used with JP6 to set compensation personality.
JP6	Y_COMP_IN	OUT	Used with JP5 to set compensation personality.
JP7	IREG_OFFSET_X	OUT	Changes X current regulator from integrator to straight gain.
JP8	X_COMP_OUT	IN	Used with JP9 to set compensation personality.
JP9	X_COMP_IN	OUT	Used with JP8 to set compensation personality.
JP10	FLASH BOOT-BLOCK PROGRAM	B (2-3) A (1-2)	Enables boot-block programming. Disables boot-block programming.
JP11	RESET	IN OUT	When present, holds the board in RESET (used for in-circuit programming & testing)

2-4 ELECTRICAL INTERFACE REQUIREMENTS

2-4-1 HSSD Fiber Optic Inputs

J1 - CLOCK (HP HFBR-2416 connector on circuit board)

J2 - X (HP HFBR-2416 connector on circuit board)

J3 - Y (HP HFBR-2416 connector on circuit board)

J4 - Z (HP HFBR-2416 connector on circuit board)

Connector #	SIGNAL NAME	DIRECTION	SIGNAL TYPE
J1	HSSD_IN_CLK	INPUT	820 nm Optical
J2	HSSD_IN_X	INPUT	820 nm Optical
J3	HSSD_IN_Y	INPUT	820 nm Optical
J4	HSSD_IN_Z	INPUT	820 nm Optical

2-4-2 MDS Fiber Optic Connectors

J5 - RXD (HP Versatile Link connector on circuit board)
J6 - TXD (HP Versatile Link connector on circuit board)

Connector #	SIGNAL NAME	DIRECTION	SIGNAL TYPE
J5	MDS_RXD	INPUT	660 nm Optical
J6	MDS_TXD	OUTPUT	660 nm Optical

2-4-3 SGA Interface

J7 - SGA X (37 position female sub-D connector)
J8 - SGA Y (37 position female sub-D connector)
J9 - SGA Z (37 position female sub-D connector)

PIN #	SIGNAL NAME	DIRECTION	SIGNAL TYPE
1/20	SGA_INTERLOCK_IN/no connect		Short to pin 19 @ SGA
2/21	SGA_GENABLE+/-	OUTPUT	RS-422
3/22	SGA_RDY+/-	INPUT	RS-422
4/23	SGA_OT+/-	INPUT	RS-422
5/24	SGA_WF_PSUV+/-	INPUT	RS-422
6/25	SGA_OC+/-	INPUT	RS-422
7/26	SGA_OV+/-	INPUT	RS-422
8/27	SGA_UV+/-	INPUT	RS-422
9/28	SGA_RESET+/-	OUTPUT	RS-422
10/29	SGA_POWER+/-	INPUT	10mA
11/30	SGA_VBUS_I_HI+/-	ANALOG INPUT	Bal. DIFFERENTIAL
12/31	SGA_HST+/-	ANALOG INPUT	Bal. DIFFERENTIAL
13/32	TRI_0+/-	ANALOG OUTPUT	Bal. DIFFERENTIAL
14/33	LDIDT+/-	ANALOG OUTPUT	Bal. DIFFERENTIAL
15/34	TRI_90+/-	ANALOG OUTPUT	Bal. DIFFERENTIAL
16/35	ICOIL+/-	ANALOG INPUT	Bal. DIFFERENTIAL
17/36	VDRIVE+/-	ANALOG OUTPUT	Bal. DIFFERENTIAL
18/37	VFILT+/-	ANALOG INPUT	Bal. DIFFERENTIAL
19	SGA_INTERLOCK_OUT		short to pin 1 @ SGA

2-4-4 SGAPS Interface

J10 - SGAPS (37 position male sub-D connector)

PIN #	SIGNAL NAME	DIRECTION	SIGNAL TYPE
1/20	SGAPS_INTERLOCK_IN/no connect		Short to pin 19 @ SGAPS
2/21	SGAPS_OC+/-	INPUT	RS-422
3/22	SGAPS_RDY+/-	INPUT	RS-422
4/23	SGAPS_OV+/-	INPUT	RS-422
5/24	SGAPS_OT+/-	INPUT	RS-422
6/25	SGAPS_WF_PSUV+/-	INPUT	RS-422
7/26	SGAPS_UV+/-	INPUT	RS-422
8/27	SR+/-	OUTPUT	RS-422
9/28	SGAPS_GENABLE+/-	OUTPUT	RS-422
10/29	SGAPS_POWER+/-	INPUT	10mA
11/30	IP_ABS+/-	ANALOG INPUT	Bal. DIFFERENTIAL
12/31	SGAPS_HST+/-	ANALOG INPUT	Bal. DIFFERENTIAL
13/37	LGND	INPUT	
14/32	SGAPS_VBUS+/-	ANALOG INPUT	Bal. DIFFERENTIAL
15/33	VLOAD+/-	ANALOG INPUT	Bal. DIFFERENTIAL
16/34	VCONT+/-	ANALOG INPUT	Bal. DIFFERENTIAL
17/35	RAD_FDBK+/-	ANALOG INPUT	Bal. DIFFERENTIAL
18/36	SGAPS_RESET+/-	OUTPUT	RS-422
19	SGAPS_INTERLOCK_OUT		Short to pin 1 @ SGAPS

2-4-5 FAN Interface

J11 - FAN (15 position female sub-D connector)

PIN #	SIGNAL NAME	DIRECTION	SIGNAL TYPE
1/6/15	no connect		
2/10	SET3+/-	OUTPUT	RS-422
3/11	SET2+/-	OUTPUT	RS-422
4/12	SET1+/-	OUTPUT	RS-422
5/13	SET0+/-	OUTPUT	RS-422
14	RELAY_DRIVER	OUTPUT	Relay Driver
7	RELAY_DRIVER_RET	OUTPUT	Relay Driver
8	Common	INPUT	GND
9	FAN_FAULT	INPUT	RS-422

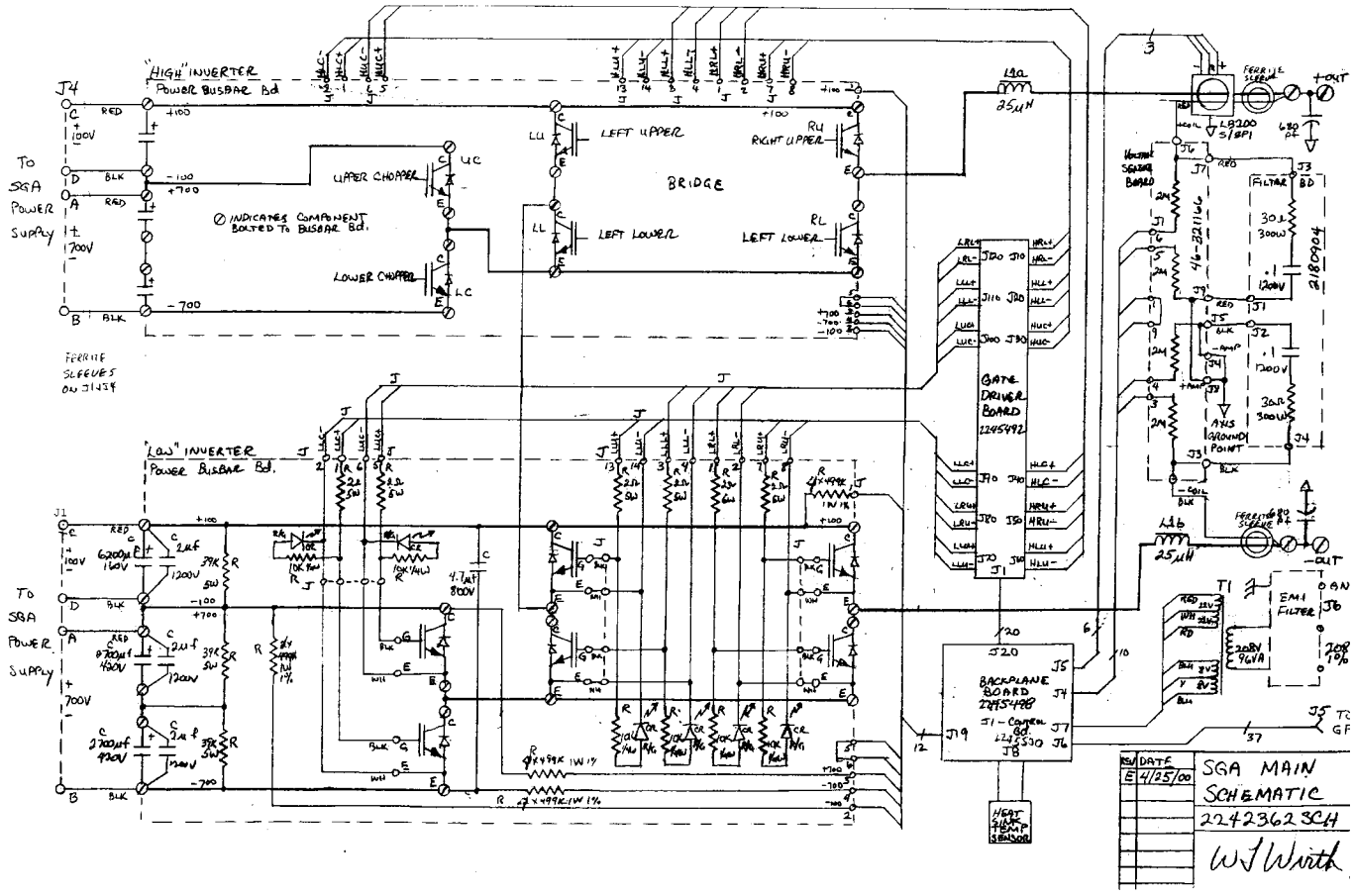
3-SWITCHABLE GRADIENT AMPLIFIER (SGA)

3-1 Description

The SGA is an IGBT based switching voltage amplifier that is part of ACGD. There are three separate identical SGA's and one power supply per ACGD system. The SGA provides the voltage and current to the gradient coil during scanning. ACGD differs from SGD in that current control during flattops is by pulse width modulation (PWM) of the SGA output bridge instead of GPM linear amplifiers.

The inputs to the SGA are voltage and current commands from the Gradient Processor Bd. (GP). The SGA has two floating outputs that are wired in series to provide the total gradient driver voltage. Also, internal to SGA is the current sensor which provides a current feedback signal to the GP.

The SGA is composed of: 2 IGBT inverters and choppers, output filters, SGA Control bd., SGA gate driver bd., Voltage Sense bd., Backplane Bd., LEM current sensors, and associated cabling / packaging. See Illustration 3-1.



SGA MAIN SCHEMATIC
ILLUSTRATION 3-1

3-2 Performance Requirements

The performance requirements for the SGA are shown in Table 3-1.

TABLE 3-1
PERFORMANCE REQUIREMENTS

Parameter	Units	Conditions
Dynamic Performance Peak Current (min)	320 A	Peak Current rating including eddy current pre-emphasis.
Inverter Bus Voltage	100/800 V	Inverter Bus Voltage (Flattop/Ramp) for each inverter
Voltage Output (min)	1400 V	Minimum Voltage Output at peak current (320 A) from both inverters.
Duty Cycle RMS Current		
T < 0.1s	320 A	Instantaneous short time maximum current
0.1< T < 1000s	100 A	Maximum time-current characteristics limited by IGBT junction temperatures as determined by Simulink model in ACGD SSDS
T > 1000s (continuous)		Minimum long term thermal limitation. May be higher as determined by the Simulink model.
Max. Ave. Power Dissapation	2.5 KW	Continuous power dissapation limit

Parameter	Units	Conditions
Power Loss Parameters per IGBT		Parameters for Simulink power loss model:
Rsat	.00175 Ohm	
	1.5 V	Slope of IGBT V-I curve
		Offset of IGBT V-I curve
	15 V	Equivalent IGBT voltage due to switching loss
Vsat	2.25 V	Chopper loss @ 700V, 31.25Khz
		Bridge loss @ 100V, 31.25Khz
	15 C/KW	
Vsw		
Ramps		Whole heatsink at 1400LFM
Flattops	100 sec	
$R_{th(hs-a)}$	10 C/KW	
(Heatsink thermal resistance)		IGBT module baseplate to heatsink with grease
$\tau_{th(hs-a)}$	10 sec	
(Heatsink thermal time constant)		
$R_{th(c-hs)}$	5.8, 14.3, 11.4 C/KW	
(IGBT case to heatsink thermal res.)		
$\tau_{th(c-hs)}$ (IGBT case to Heatsink thermal time constant)	.003, .06, 1 sec	3 internal IGBT Rtheta, TC pairs
$R_{th(j-c)}$ (Junction to IGBT case thermal res.)		
$\tau_{th(j-c)}$ (Junction to case thermal time constants)		
Output Fidelity		
Voltage Bandwidth (min)	7 KHz	-3dB Bandwidth at full power

3-2 Current Sensor

The performance requirements for the current sensor are listed in Table 3-2.

TABLE 3-2
CURRENT SENSOR PERFORMANCE REQUIREMENTS

Parameter	Value	Units	Conditions
Measuring Range	+/-400	A	
Gain	40	A/V	
Current Offset	+/-1.5m	A	+10 to +50 C
Linearity	.1%	%	
Bandwidth	150k	Hz	-1dB

3-3 Error Conditions

The error conditions described in Table 3-3 shall cause a Fault to occur and the SGA to shut down (come out of READY).

TABLE 3-3
ERROR CONDITIONS

Fault	Error	Signal Name	Comments
Over Current	I > 400 A	OCINST	Current at +Coil Output
Average overcurrent	I>135A/20sec	OCAVG	RMS higher/depends on PSD
Over Voltage	V > 850 V	OV	Input voltage on Chopper
Under Voltage	V < 50 V	UV	Input voltage on LV bus cap
Wiring fault		Wire	Cable or PCB not connected
Heat Sink Over Temp	T > 75 C	HSOT	IGBT Heatsink Temp.
IGBT Junction Over Temp	T > 105 C	TJMAX	Using analog simulator
Low voltage PS Undervoltage	+15V: V < +10 V -15V: V > -10 V +5V: V < +3 V +15GD: V<12V IGD: I>5Amps	PSUV	Monitors Control Bd. PS voltages and gate driver current

3-4 MECHANICAL REQUIREMENTS

3-4-1 SGA Chassis

Dimensions

The dimensions of the SGA chassis are 17” W x 8” H x 25” L.

3-4-2 Connectors

External Connectors

Connectors mating external to the SGA are listed in Table 3-4. They are located on the rear panel of the SGA chassis.

TABLE 3-4
EXTERNAL SGA CONNECTORS

Connector Name	style	to / from	Comments
Control	37 pin sub-D	GP	
Inverter Outputs: +Coil / -Coil	1/2" stud	Coil	
DC High Voltage Power	(Amphenol - MS type)	SGA-PS	2 connectors/ 700V/100V
AC Power	208V 1 phase	PDU	P<100W

Control Board LEDs

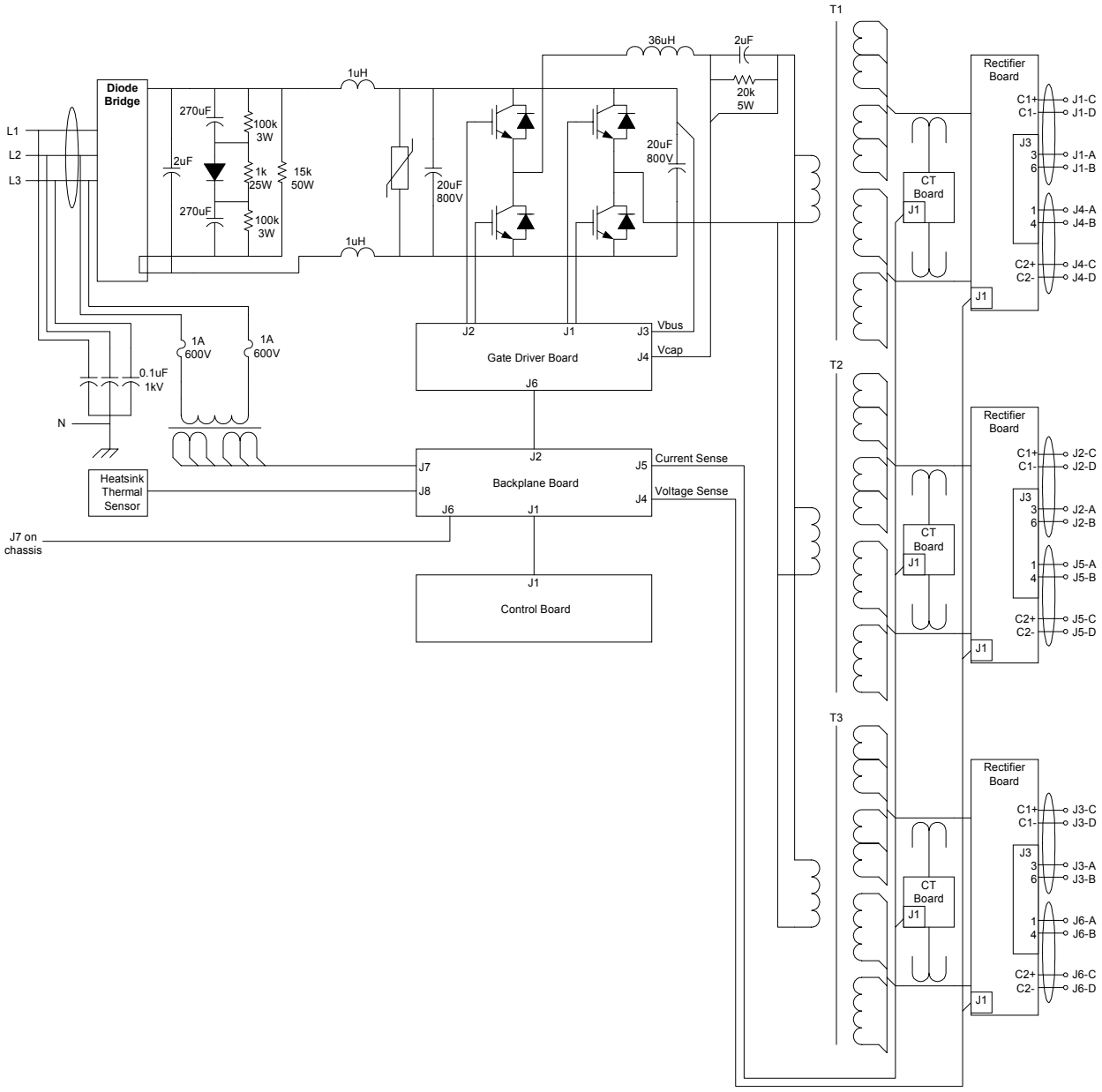
TABLE 3-5
SGA LEDS

LED	NAME	COLOR	DESCRIPTION	Visible
DS1	Vfilt/Icoil	Yel/Grn	Intensity proportional to Vfilt/Icoil. Yel pos/Grn neg	External
DS2	Ocinst/OCave	Orange	Indicates instantaneous/Average overcurrents	External
DS3	TJOT/HSOT	Orange	Indicates Junction/HeatSink overtemperatures	External
DS4	UV/OV	Orange	On indicates undervoltage/Overvoltage fault	External
DS5	WireFault/PwrSup UV	Orange	Indicate disconnected Connector/PSundervoltage	External
DS6	Chopper Gate Drivers	Yel/ Green	Indicates Chopper gate drivers active	External
DS7	H Gate Drivers	Yel / Green	Indicates H inverter gate drivers active	External
DS8	L Gate Drivers	Yel / Green	Indicates L inverter gate drivers active	External
DS10	Enable/Fault	Green	Indicates SGA enabled/SGA faults	External
DS11	GEN	Red	On indicates GP not enabling SGA	Internal
DS12	Reset	Red	On indicates GP not resetting SGA	Internal
DS12	GateDrvPS/Tj	Yel/Gree n	Indicates GDPS active/Junct tmp(Grn cold/yel hot)	External

4- SGA POWER SUPPLY

The SGA-PS (Switching Gradient Amplifier Power Supply) is an IGBT based resonant power supply. The SGA-PS has 12 floating DC outputs that supply power to the X, Y and Z axis SGAs. Each axis is supplied with two 100 VDC and two 700 VDC supplies. The 100 V supplies are rated at 50A and the 700 V supplies are rated at 12A.

The SGA-PS is composed of: an input rectifier diode bridge, an IGBT inverter, tank capacitor, tank inductor, three transformers, output filters, control board, gate driver board, backplane board, three rectifier filter boards, and all the associated cabling and packaging.



POWER SUPPLY SCHEMATIC
ILLUSTRATION 4-1

4-1 PERFORMANCE REQUIREMENTS

4-1-1 SGA Power Supply

The performance requirements for the SGA-PS are shown in Table 4-1:

TABLE 4-1
SGA-PS PERFORMANCE REQUIREMENTS

Parameter	700 V Outputs	100 V Outputs	Units	Conditions
Dynamic Performance				
Output Voltage				Applies when only one axis is loaded.
No Load Voltage	700+/-20	100 +/-20	V	@ 0% output current
Nominal Voltage	700+/-20	75+20,-0	V	@ 100% output current.
Transient Voltage Dip	650@24A	75@200A	V	Min voltage after load application.
Transient Voltage Overshoot	725	125	V	Max voltage after transient load removal.
Output Current				
Continuous Load	12	50	A	One axis loaded at a time.
Momentary Load (100 ms)	24	200	A	100V output may droop to 75 V under load.
Total Output Power				
Continuous	22.5		KW	At 100% load
Input Power				
Continuous Power	25		KVA	Maximum continuous power draw
Peak Instantaneous Power (max) < 5 sec	50		kVA	Maximum power draw for 5 seconds.
SGA-PS Loss Parameters				
Power Disspation	1500		W	Max dissipation @30kW output
Input Voltage				
Amplitude at 50/60Hz	420		V	3 phase Input AC line voltage.
Voltage Fluctuation	+10,-10		%	Maximum fluctuation of input line.
Phase Imbalance	3%		%	Maximum imbalance of input line.
Input Impedance	6%		%	Maximum total souce impedance.

4-1-2 Error Conditions

The error conditions described in Table 4-2 shall cause a Fault to occur and the SGA-PS to shut down (come out of READY). These conditions are hardware protection limits and should not be used as system capability models.

TABLE 4-2
ERROR CONDITIONS

Fault	Error	Signal Name	Comments
Over Current	I > 225 A	IPX_OC	Primary Current in the X axis Over Current
Over Current	I > 225 A	IPY_OC	Primary Current in the Y axis Over Current
Over Current	I > 225 A	IPZ_OC	Primary Current in the Z axis Over Current
Over Current	I > 525 A	I_TANK_OC	Over Current in the Tank
Over Current	I > 60 A for 700V supply I > 250 A for 100V supply	ISX_OC	Secondary Current in the X axis Over Current
Over Current	I > 60 A for 700V supply I > 250 A for 100V supply	ISY_OC	Secondary Current in the Y axis Over Current
Over Current	I > 60 A for 700V supply I > 250 A for 100V supply	ISZ_OC	Secondary Current in the Z axis Over Current
Over Voltage	700 V supply > 800 V	OVX	Over Voltage in the Secondary X axis
Over Voltage	700 V supply > 800 V	OVY	Over Voltage in the Secondary Y axis
Over Voltage	700 V supply > 800 V	OVZ	Over Voltage in the Secondary Z axis
Over Voltage	V > 850 V	OVBUS	Over Voltage in the BUS
Under Voltage	700V supply < 400 V 100V supply < 50 V	UVX	Under Voltage in the Secondary X axis
Under Voltage	700V supply < 400 V 100V supply < 50 V	UVY	Under Voltage in the Secondary Y axis
Under Voltage	700V supply < 400 V 100V supply < 50 V	UVZ	Under Voltage in the Secondary Z axis
Under Voltage	V < 300 V	UVBUS	Under Voltage in the BUS
Over Temperature	T > 75 C	HSOT	Heat Sink Over Temp
Over Temperature	T > 125 C	TJMAX	IGBT Junction Over Temp. TBD analog simulator
Wire Fault		WF	Wire Fault interconnection
Low voltage PS Undervoltage	+15V supply < 12 V +15GD supply < 12 V	PSUV	Monitors Control Bd. PS voltages

4-2 Electrical Interface Requirements

4-2-1 GP Interface, J7

J7 PIN #	SIGNAL NAME	DIRECTION	SIGNAL TYPE
1	SGA-PS_INTERLOCK_IN		Short to pin 19 on board
21/2	SGAPS_OC+/-	OUTPUT	RS-422
3/22	SGAPS_RDY+/-	OUTPUT	RS-422
23/4	SGAPS_OV+/-	OUTPUT	RS-422
24/5	SGAPS_OT+/-	OUTPUT	RS-422
25/6	SGAPS_WF_PSUV+/-	OUTPUT	RS-422
26/7	SGAPS_UV+/-	OUTPUT	RS-422
8/27	SR+/-	INPUT	RS-422
9/28	SGAPS_GENABLE+/-	INPUT	RS-422
10/29	SGAPS_POWER+/-	OUTPUT	10mA
11/30	IP_ABS+/-	ANALOG OUTPUT	RS-422
12/31	SGAPS_HST+/-	ANALOG OUTPUT	Bal. DIFFERENTIAL
13/37	LGND	OUTPUT	
14/32	SGAPS_VBUS+/-	ANALOG OUTPUT	Bal. DIFFERENTIAL
15/33	VLOAD+/-	ANALOG OUTPUT	Bal. DIFFERENTIAL
16/34	VCONT+/-	ANALOG OUTPUT	Bal. DIFFERENTIAL
17/35	RAD_FDBK+/-	ANALOG OUTPUT	Bal. DIFFERENTIAL
18/36	SGAPS_RESET+/-	INPUT	RS-422
19	SGAPS_INTERLOCK_OUT		Short to pin 1 on board
20	No Connect		

4-2-2 SGA X_Y_Z Interface

PIN #	SIGNAL NAME	DIRECTION	SIGNAL TYPE
J1-A/B	X axis Low side 700V supply	OUTPUT	POWER
J1-C/D	X axis Low side 100V supply	OUTPUT	POWER
J4-A/B	X axis High side 700V supply	OUTPUT	POWER
J4-C/D	X axis High side 100V supply	OUTPUT	POWER
J2-A/B	Y axis Low side 700V supply	OUTPUT	POWER
J2-C/D	Y axis Low side 100V supply	OUTPUT	POWER
J5-A/B	Y axis High side 700V supply	OUTPUT	POWER
J5-C/D	Y axis High side 100V supply	OUTPUT	POWER
J3-A/B	Z axis Low side 700V supply	OUTPUT	POWER
J3-C/D	Z axis Low side 100V supply	OUTPUT	POWER
J6-A/B	Z axis High 700V supply	OUTPUT	POWER
J6-C/D	Z axis High 700V supply	OUTPUT	POWER

4-2-3 Power Supply Terminal strip, J7

J7 POS #	SIGNAL NAME	DIRECTION	SIGNAL TYPE
J7-1	420 VAC	INPUT	POWER
J7-2	420 VAC	INPUT	POWER
J7-3	420 VAC	INPUT	POWER

REVISION HISTORY

REV	DATE	AUTHOR	PRIMARY REASONS FOR CHANGE
A	Sept. 11, 2000	K. Keshena	Preliminary version.
0	Oct. 20, 2000	K. Keshena	Initial release.