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Description - This document combines all theory files that are relative to Signa Horizon Lx systems with 8645/GRAM gradient driver.

1- GRADIENT DRIVER SUBSYSTEM OVERVIEW

Description - *Gradient driver system* is a new designation that refers to the entire gradient power delivery method. It applies to the GRAM cabinet and the 8645 gradient cabinet.

1-1- Overview

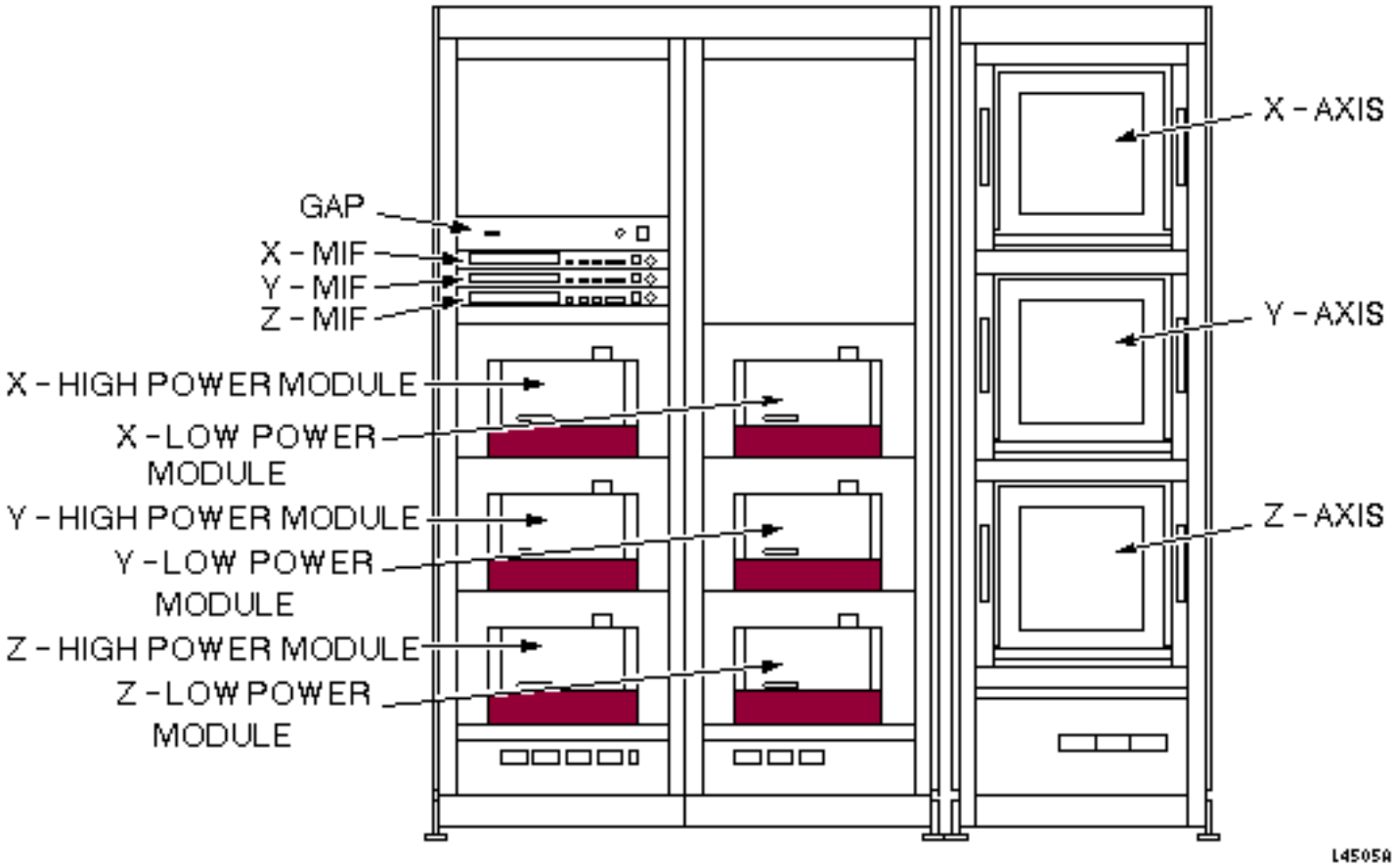
Portions of the UFI system include the following hardware:

- IPG board: slight modifications to the existing board
- Gradient Amplifier Processor (GAP) board
- Master interface (MIF) board
- Power module: peak current ±200 amperes
- Gradient Ramp Accelerator Module (GRAM)
- New gradient filter box and cables
- Water-cooled epoxy-filled gradient coil
- PDU circuit breakers for GRAM and 8645
- Analog Service Module (ASM) board
- GRAM Analog Service Module (GASM) board
- Blower box
- Heat exchanger

1-2 - Gradient Amplifier Cabinet

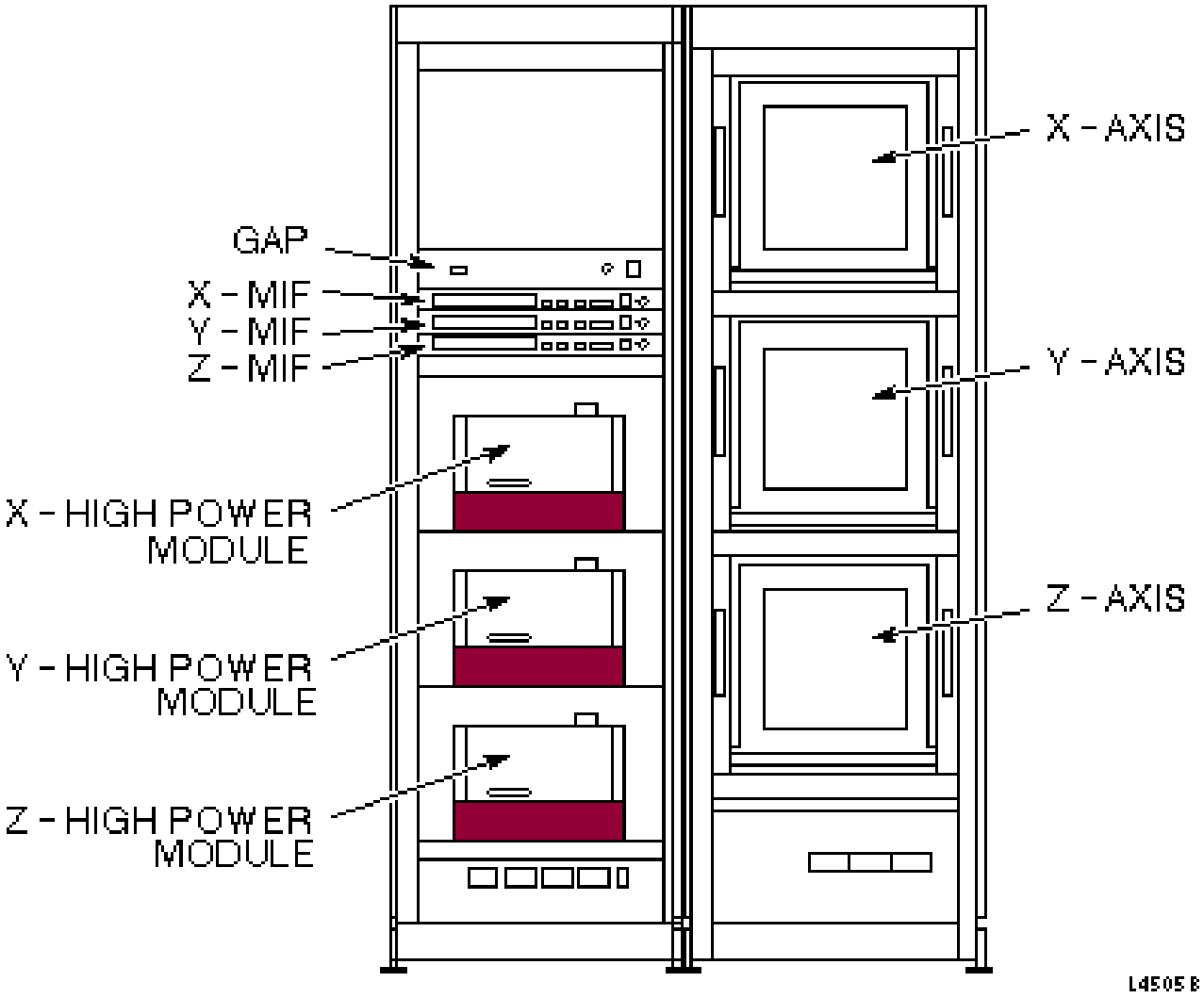
The 8645 power modules are all the same. They are now separated as Hi and Low Power Modules (the power modules are now referred to as Hi/Low Power Modules, versus the old terminology of *master* and *slave* amplifiers). The control circuitry that once was enabled on the master amplifiers is now on the MIF board in the 8645 gradient amplifier cabinet. The same circuitry existed on the 8607 slave, but was disabled, adding extra cost to the system. One MIF board is needed per axis. See one of the following illustrations, depending on which system you are servicing:

- Signa Horizon EchoSpeed Illustration L4505A.



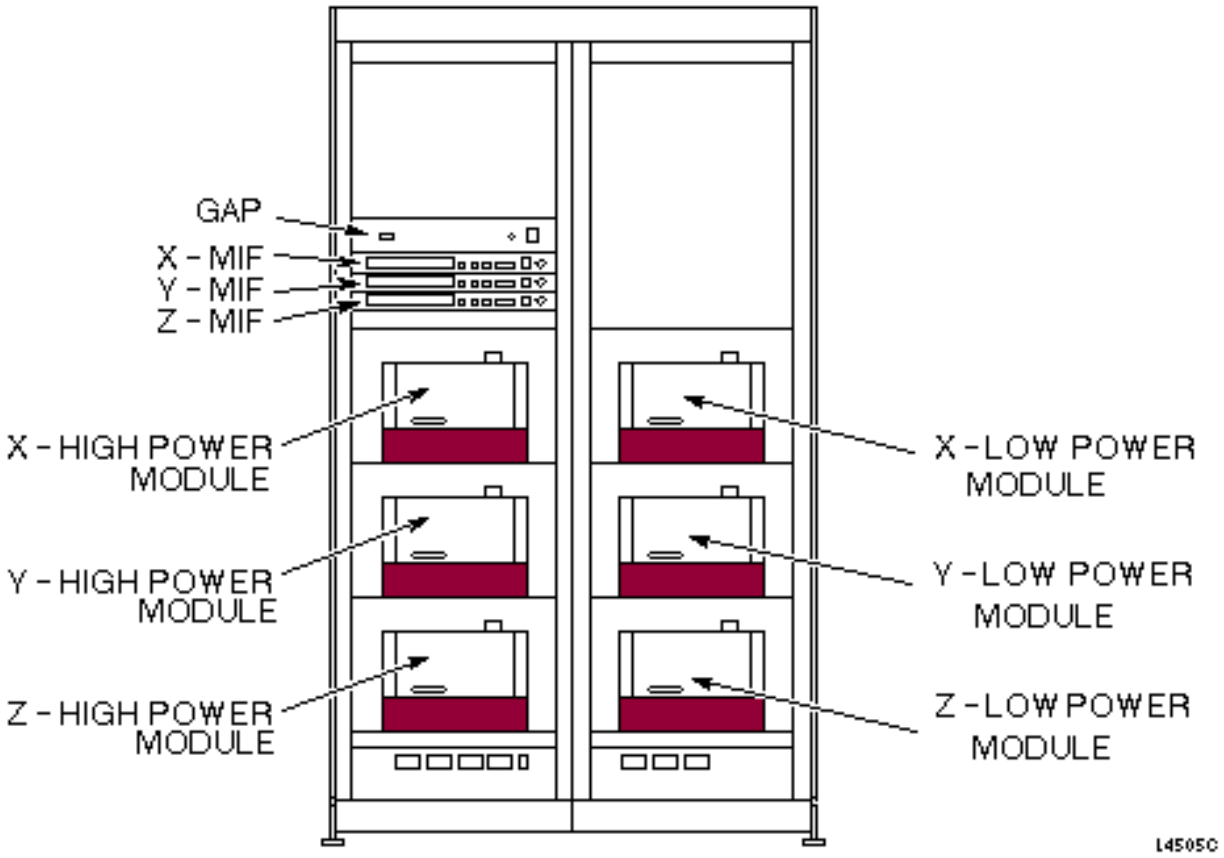
8645 GRAD AMP & GRAM CABINETS, SIGNA HORIZON ECHOSPEED: FRONT VIEW
ILLUSTRATION L4505A

- Signa Horizon HiSpeed Illustration L4505B.



8645 GRAD AMP & GRAM CABINETS, SIGNA HORIZON HISPEED: FRONT VIEW
ILLUSTRATION L4505B

- Signa Horizon Illustration L4505C.

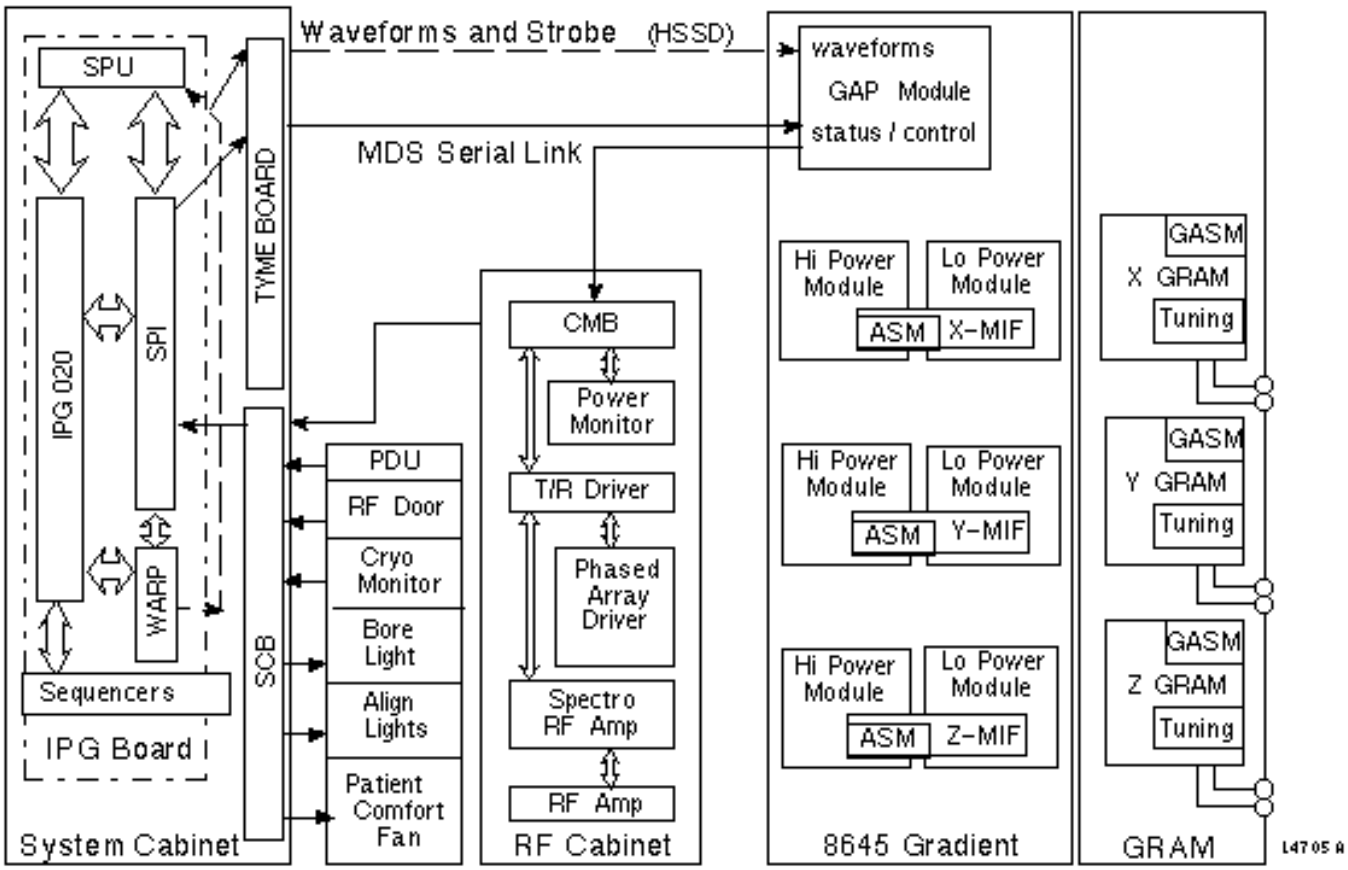


8645 GRAD AMP & GRAM CABINETS, SIGNA HORIZON: FRONT VIEW
ILLUSTRATION L4505C

1-3- Gradient Driver Block Diagrams

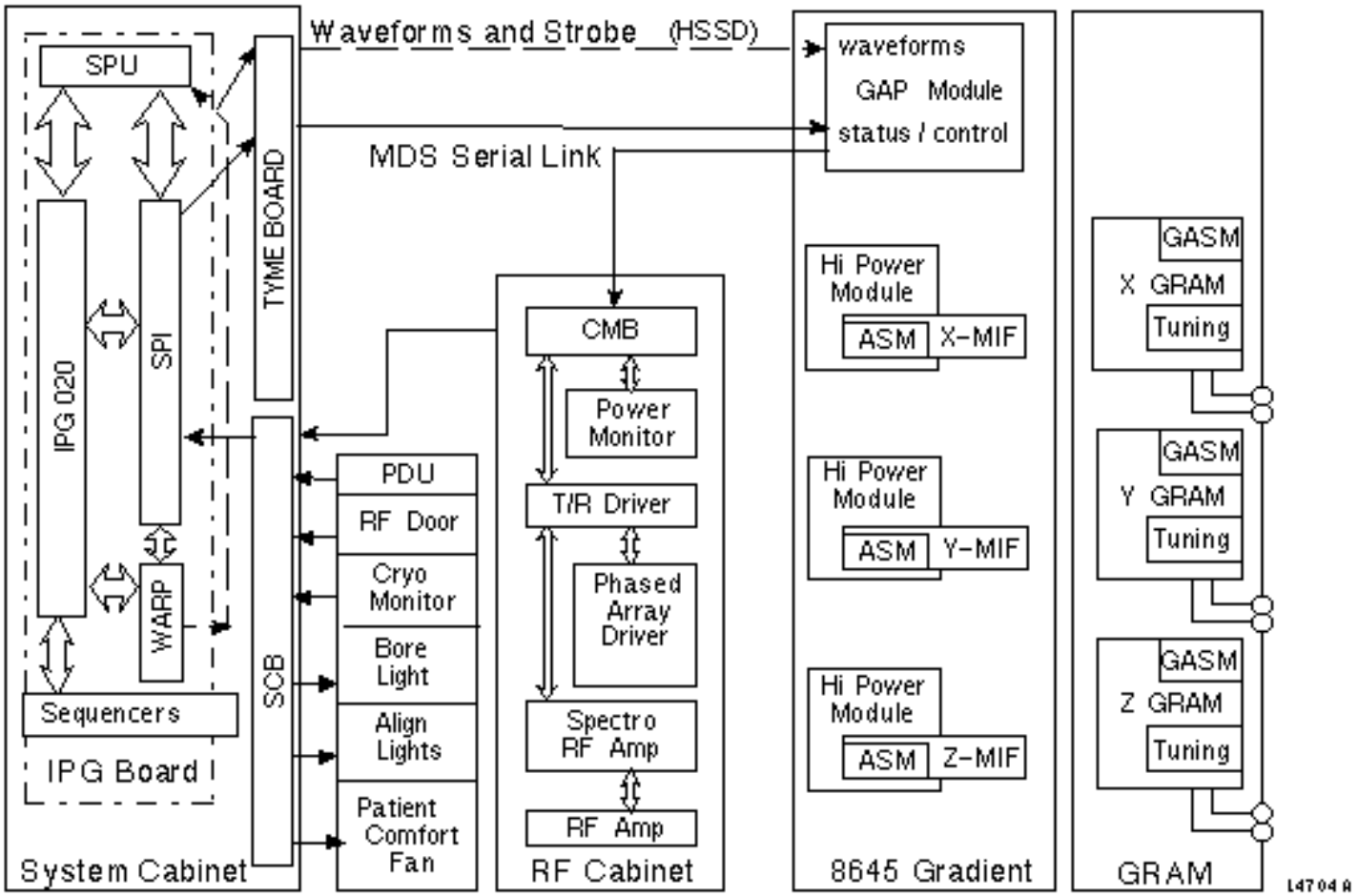
There are three gradient driver system configurations to support the Signa Horizon offerings:

- Signa Horizon EchoSpeed block diagram Illustration L4705A.



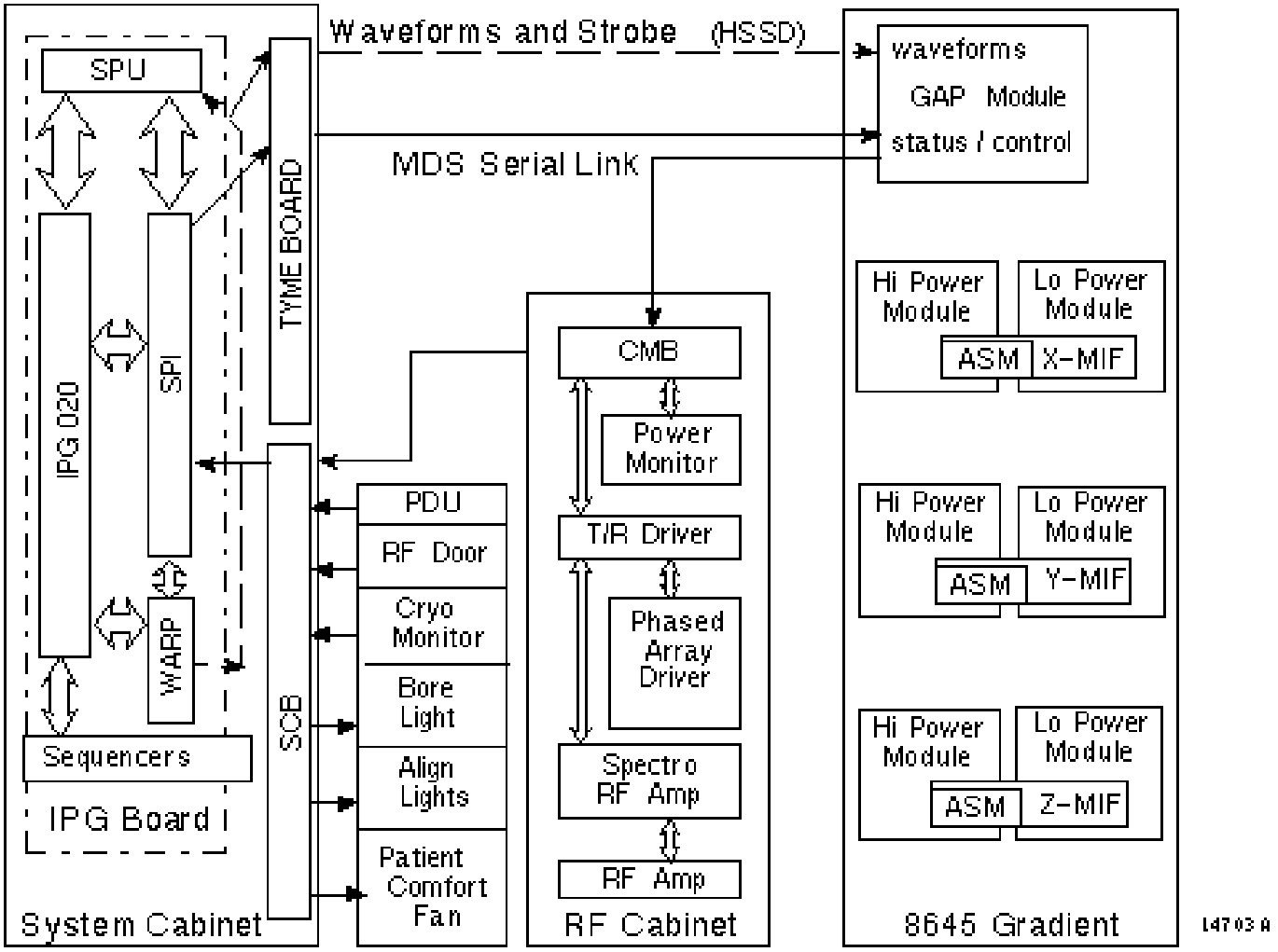
SIGNA HORIZON ECHOSPEED GRADIENT BLOCK DIAGRAM
ILLUSTRATION L4705A

- Signa Horizon HiSpeed gradient block diagram Illustration L4704A.



SIGNA HORIZON HISPEED GRADIENT BLOCK DIAGRAM
ILLUSTRATION L4704A

- Signa Horizon gradient block diagram Illustration L4703A.



SIGNA HORIZON GRADIENT BLOCK DIAGRAM
ILLUSTRATION L4703A

1-3-1 Communication Over MDS Link to IPG Board

The MDS (multidrop serial) link presently connects the GAP board and the TPS chassis. It is used to receive/send status commands to the amplifiers, report errors, and to pass any other information to the operator, or service person. The function of the MDS link has not changed with this new hardware; however, there is no bicycle link with the new hardware.

Note

New component names - The number 8645 refers only to the gradient amplifier cabinet, not to the new power modules. Since the control circuitry is now on the MIF boards, what once were called the gradient amplifiers are now called power modules

1-3-2 GAP Board

The GAP board and the IPG board control the state of the amplifiers. The GAP board controls and is responsible for reporting status of all peripherals in the gradient driver subsystem for each axis:

- Gradient state (ready/standby)
- Gradient overload reset
- Reset data errors
- GRAM mode – GRAM status monitoring, GRAM control (error reporting/handling)
- Load Compensation. This is affected by the resistance and inductance of the coil, thus it will change between head, body, and surface coils.
- Full Scale
- Gradient fan speed control

Note

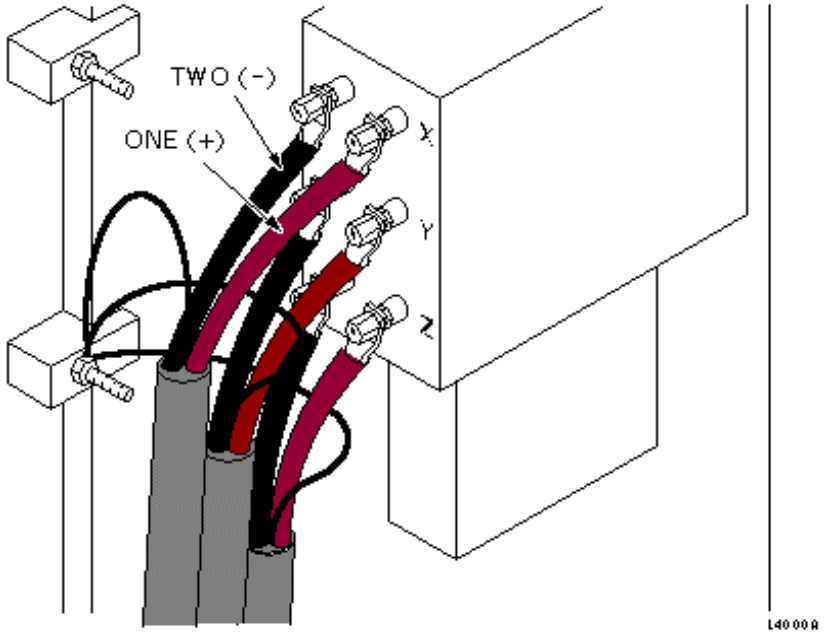
Power module control - For systems with two power modules per axis, the power modules are always controlled together. It is not possible to change the state of the one without changing the other

1-3-3 Gradient Output Cables

The gradient output cables are noticeably different from those used in current Signa product. They are constructed of 10 AWG stranded wire, rather than the 8 AWG used currently. This cable is rated for 2000 volts from one conductor to ground. The cable has a rating of 217 amperes, which is the amount of current that the cable can handle and not exceed 90º C. Coil resistance is 0.0238 ohms over a 200-foot path, from the gradient amplifier, to the coil, and back again. The cable weighs about two pounds per foot, and can be difficult to route. Allocate more time to the placement and routing of this cable than you would to route current product.

1-3-4 Gradient Filter Box

The gradient filter box is designed to handle 200 amperes and 2000 volts. It has 1/2-inch diameter lugs on it for the heavier gauge cable see Illustration L4000A.



GRADIENT FILTER BOX
ILLUSTRATION L4000A

2- IPG BOARD MODIFICATIONS FOR SIGNA HORIZON

The material in this section applies to Signa Horizon systems from release 8.0 forward.

Description - The IPG board has been modified for Signa Horizon in order to accommodate the new gradient hardware. WARP software, SRI PROMs, SCB PROMs, the `ipg_stage` file, configurable SPI files, and SPU software have all had changes made to them.

2-1- WARP Software

WARP (waveform rotational processor) software has been modified to accommodate FRESBECC and Digital Eddy Current Compensation, necessary for the Signa Horizon product. The Grafidy kit, Grafidy analysis tool, and Grafidy PSD are used to analyze linear and B_0 eddy currents that are present. Compensation values are calculated, and downloaded to the IPG board.

For a complete discussion of eddy current compensation, see the procedure for Eddy Current Compensation Theory.

2-1-1 FRESBECC and WARP

The WARP software has been modified to handle the calculations necessary for FRESBECC, which means *frequency shift B_0 eddy current compensation*. It allows B_0 eddy currents to be compensated for via the software. This signal is sent to the exciter, which also has hardware modifications for B_0. FRESBECC is sometimes referred to as *digital B_0*. It is performed on all systems that have 8645 gradient amplifier cabinets.

2-1-2 Digital Eddy Current Compensation and WARP

The base Signa Horizon product has neither a GRAM, nor a tuning board. Linear long eddy currents are compensated for in the WARP. Digital eddy current compensation, using the eddy current compensation program, Grafidy, is performed only on the Signa Horizon configuration.

2-1-3 IPG Downloads Files To WARP

The IPG application code downloads files to WARP when you go to the Scan Operations page, or when you select **[Download]** on the Scan Operations page. This is called a *CV download*. One of the files that is downloaded to WARP is the `ecccoeff.dat` file. This file generates the digital B_0 coefficients for all Signa Horizon products, and digital eddy current coefficients for Signa Horizon only when these calibrations are run. The first time that the system is installed, or a load from cold is performed, or software is upgraded, a message states that this file has not been created:

```
2225061
"IPG Advisory message – DECC will not be performed during scanning.
Eddy Current Compensation coefficient file /usr/g/caldir/ ecccoeff.dat
could not be found or could not be opened. Please run Grafidy to create
the file."
```

This does not prevent scanning; however; it indicates that eddy current compensation must be performed on the system. These calibrations are necessary in order to generate the `ecccoeff.dat` file.

2-2- IPG Downloads Files to GAP

The IPG application code downloads the `gram_tune.dat` file to GAP when you download CVs, if a GRAM and a digital tuning board are sensed and present. The `gram_tune.dat` file contains the digital coefficients necessary for providing eddy current compensation on the digital tuning board. This file does not exist until the eddy current compensation portion of the GRAM tuning procedure is performed on the digital tuning board. If this file is not present, an error is reported to the message log:

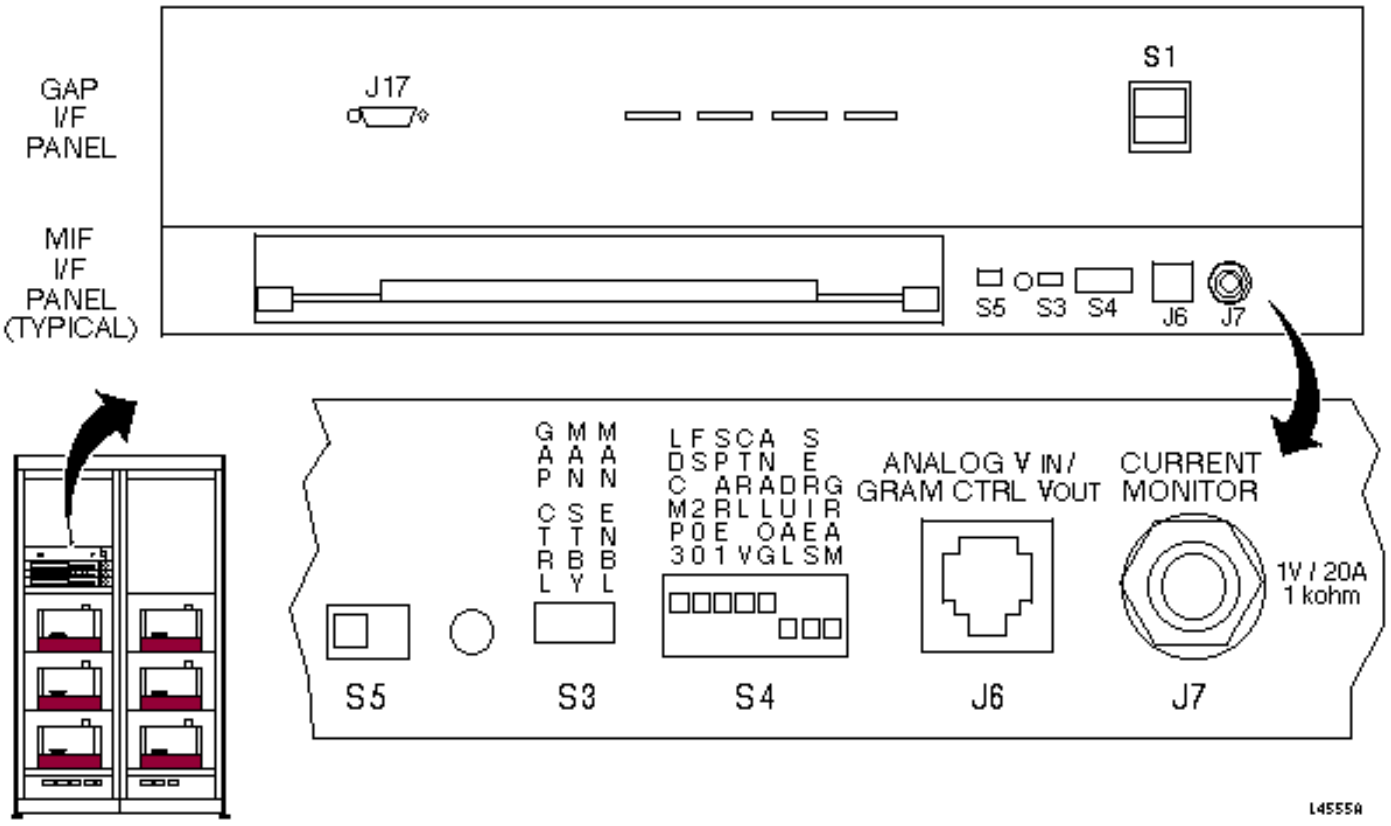
```
2225007
"IPG Advisory Message
IPG could not open the gram_ tune.dat file in /usr/g/caldir.
Please do restore info or run Grafidy to create the file."
```

This does not cause the system to crash; however, it indicates that GRAM tuning must be performed on the system. This calibration is necessary in order to generate the `ecccoeff.dat` file.

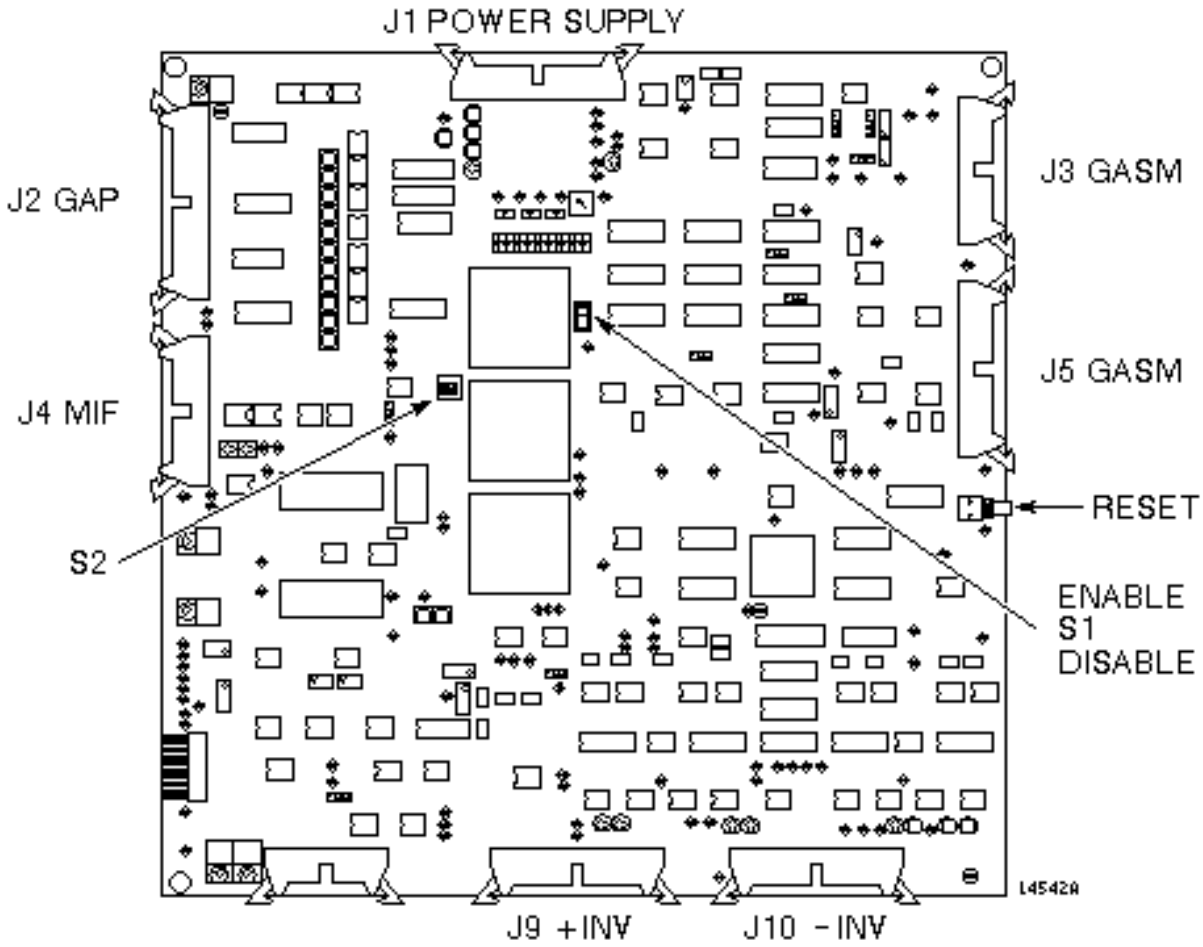
2-3- The ipg_stage File

The `ipg_stage` file includes emulation of the gradient driver subsystem, including the power modules and GRAMs (if present). When *G* is entered in the first line of `ipg_stage`, SPI does not send commands to the gradient amplifiers, and does not monitor their state; therefore, the gradient amplifiers remain in standby mode, so there can be no output from them. On a system with 8645 power modules, the gradient configuration will still be downloaded. Real-time monitoring is not performed if enabled in the `MRconfig.cfg` file. If the system has GRAMs, digital tuning values are downloaded if digital tuning boards are selected in the `MRconfig.cfg` file.

The gradients should be placed in manual standby, or manual ready by the three-position switch, S3, on the front of the gradient cabinet see Illustration L4555A. GRAMS should have S1, the Enable/Disable switch in the *enable*, or *up*, position, and S2, the four-switch dip switch should have the right-most switch in the *manual control mode* see Illustration L4542A.



MIF FRONT PANEL DISPLAY
ILLUSTRATION L4555A



GRAM I CONTROL BOARD - SWITCHES AND JUMPERS
ILLUSTRATION L4542A

2-4- IPG Hardware Modifications

IPG boards support digital B_0 compensation. This allows the IPG board to communicate information to the exciter board with frequency adjustments to compensate for B_0 eddy currents.

3- GAP BOARD

Description - GAP is an acronym for Gradient Amplifier Processor. The GAP board is one of the three nodes on the MDS link; it replaces the SPG and gradient Interface board.

3-1- Overview

The GAP is resident in the 8645 gradient amplifier cabinet, and serves as the command interface between the gradient driver subsystem and the IPG/TPS cabinet. The MDS link is the physical interface between the GAP board and the IPG board in the TPS chassis. The GAP microprocessor is a Texas Instruments 320C31 digital signal processor (DSP). This processor was chosen for its digital filtering capability and its low cost. GAP interprets system commands and provides low-level control and monitoring of the power modules. If analog service modules (ASMs) are present on any or all power module axes, or GRAM analog service modules (GASMs) are present on any or all GRAMs, then GAP can monitor voltages, currents, and temperatures of the power modules or GRAMs (if present).

Note

When GRAMs are present - GRAMs are present on each axis for Signa Horizon EchoSpeed and Signa Horizon HiSpeed systems only. Signa Horizon systems do not have GRAMs

3-2- Functional Description

3-2-1 Gradient State Control

GAP software controls and monitors the state of the 8645 power monitors and GRAMs (if present). Normal state transitions are initiated by the IPG/TPS system. GAP interprets MDS control commands from the system, and performs register operations necessary to carry out the command. GAP always takes current configuration into account when responding to a state change request. GAP monitors state transition timing to ensure proper operation. Improper state transitions are reported to the system.

3-2-2 Amplifier Status Monitor

The GAP application code monitors the status of the power modules at all times. While in standby mode, all register status bits are continuously read. While in the ready mode, the real-time status signals are monitored with circuitry that produces a processor interrupt when a state change occurs. The intent is to avoid reading registers during scanning since it may induce electrical noise and subsequently degrade image quality. Inappropriate status at any time is reported to the system via the MDS link.

3-2-3 MDS Interface

The GAP board functions as an MDS slave node. TPS/IPG controls the gradient driver subsystem via MDS packets. Likewise, status information is passed back to the system via the MDS link. MDS communication is coordinated by the SPI processor on IPG. GAP responds to all packets from the SPI. GAP does not initiate MDS communications except under certain error conditions in which the GAP does not receive MDS communication.

3-2-4 Software Download

Each time the GAP board is reset, the boot code executes and performs diagnostic tests of the DUART, external static RAM, and checksum of the application code in flash memory on the GAP board. After successful completion of the DUART, external static RAM tests, pass or failure of the checksum test, and MDS initialization, the GAP board is ready to communicate with SPI. SPI requests the GAP file header packet from GAP. This packet consists of the time-stamp, version, file length, and checksum of the file stored on the GAP board.

If any of these differs from the time stamp, version, file length, and checksum of the GAP application file on the host, the file on the host is downloaded over the MDS link to external static RAM on GAP. The code is then copied from external static RAM on the GAP board to flash memory on the GAP board.

3-2-5 Fan Speed Control

The GAP application code sets the fan to low speed upon reset. All other control of the fan speed is initiated externally. An MDS command opcode is available, which allows the fan logic to be implemented on the SPI. The SPI commands the fan to high speed when the SPI commands the gradients to the ready mode, and to low speed when the SPI commands the gradients to standby. All other GAP processing is independent of fan speed.

3-3- Gradient Controller State Transitions

The GAP software controls and monitors the state of the 8645 power modules and the GRAM (if present). Axis states are independent of each other. The state controller actually consists of three independent state machines running in parallel. These are defined below.

3-3-1 RESET_INIT

This is the initial state of the controller after a power-up, or reset condition, when the axis has a GRAM. The controller remains in this state for 1.5 seconds, the reset time of the GRAM. After 1.5 seconds, the state changes to INIT.

3-3-2 INIT

This is the initial state of the controller after a power-up, or reset condition, when the axis does not have a GRAM. The controller remains in this state until the amplifier and GRAM (if present) are in a proper state . If a GRAM is present, then the *inverter ready* and *controller ready* must be true before going to the standby mode.

3-3-3 Standby

The controller is in this state whenever the amplifier and GRAM (if present) indicate standby status. While in this state, registers on the MIF board and GRAM are polled periodically. Time-out for this state is set to one second.

3-3-4 Recovery

The controller is in this state until no faults exist on the GRAM or the MIF board. Time-out is set to one second. If the faults do not go away, the time-out is again set to one second, and the controller remains in this state, monitoring faults. If a GRAM fault exists after the one-second time-out, the state changes to Reset.

3-3-5 Reset

Whenever a GRAM fault is detected, the GRAM is reset and the axis controller is put in this state. Axis status is not monitored while in this state. This state times out in 1.5 seconds, then changes to Recovery, and then to Standby.

3-3-6 Lag

When all three axes are requested to go to Ready simultaneously, the *y* and *z* axes controllers are put into this state to delay the actual issue of the ready command to these axes. Axis status is not monitored while in this state. This state times out in 50 milliseconds for the *y* axis, and 100 milliseconds for the *z* axis. This state does not exist for the *x* axis. When the state times out, the axis is requested to go to Ready.

3-3-7 GOING_READY

When the ready command is issued to the axis, the controller enters this state to monitor the transition to the Ready state. This state is necessary since it takes the hardware up to 750 milliseconds for this transition. Actual time-out of this state is set to one second. This state terminates when the axis status indicates Ready status, or when the timeout occurs. An error is logged if this time-out expires, and the axis is requested to go to standby. Axis status is not directly monitored while in this state; however, any fatal error would prevent the axis from indicating Ready status, which would cause a state time-out to occur.

3-3-8 READY

The controller is in this state whenever the axis status is Ready. This state terminates only when the axis is commanded to Standby, or when a fault (other than overload) occurs.

3-3-9 GOING_STANDBY

When the Standby command is issued to the axis, the controller enters this state to monitor the transition to the Standby state. This state is necessary since it takes the hardware up to 15 milliseconds for this transition. Actual time-out of this state is set to one second. An error is logged if the state time-out expires and the state is set to GOING_READY. An error is logged if a fault is detected, and the state is set to Recovery if there are no GRAM faults, or to Reset if there is a GRAM fault.

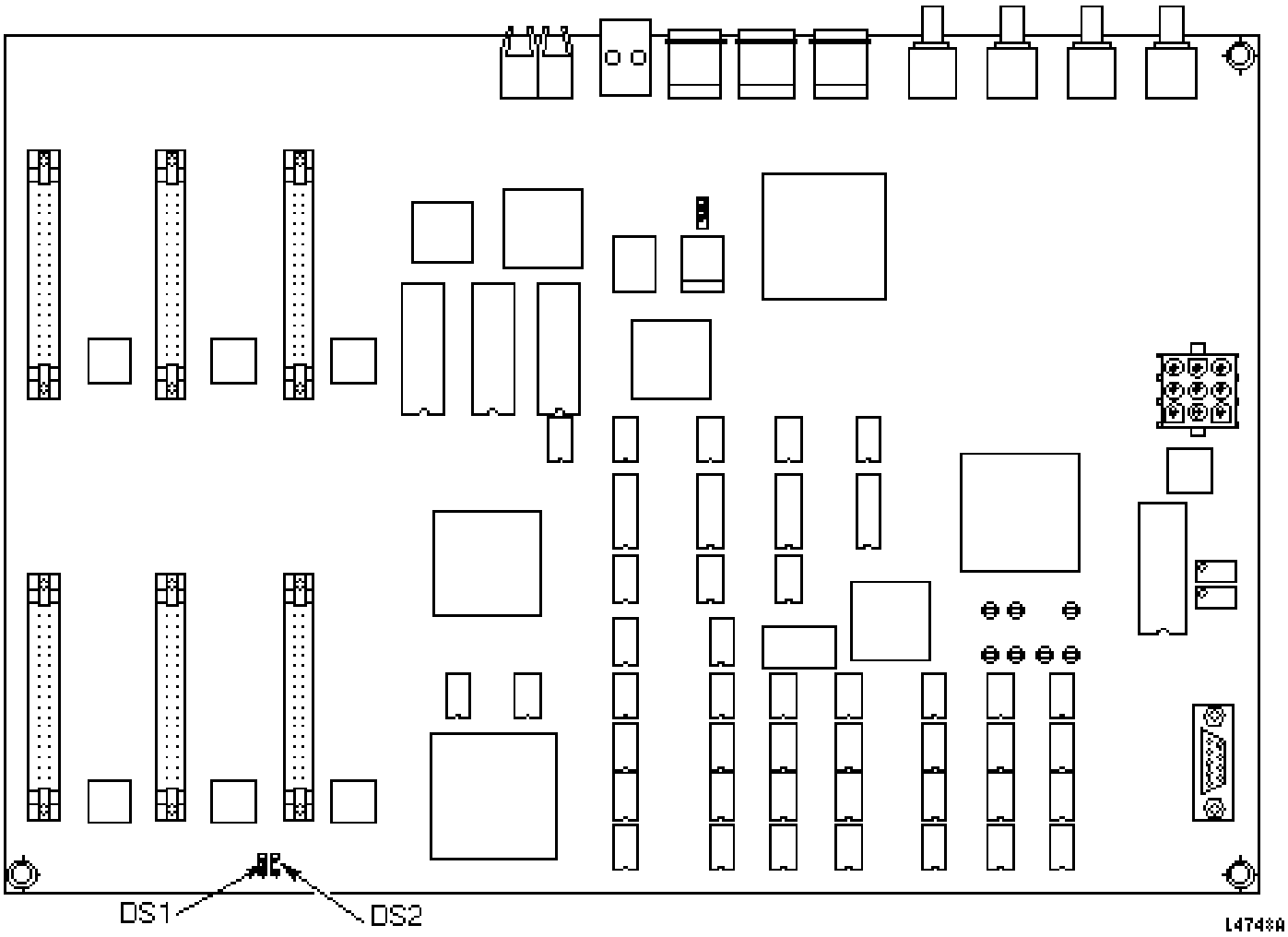
3-4- GAP Status LEDs

The GAP board has two status LEDs: DS1 and DS2. DS1 is always on when the GAP board has power. DS2 provides status information. During normal use, DS2 flashes on and off with a period of five seconds, and a fifty percent duty cycle, to indicate that the GAP board is executing code. During boot code execution, DS2 flashes if there is an error with the DUART, or the external static RAM on the GAP board. An error with the DUART causes DS2 to flash on and off with a period of one second with a fifty percent duty cycle. An error with the external static RAM causes DS2 to flash on for one quarter of a second, flash off for one quarter of a second, flash on for a quarter of a second, and then flash off for one half of a second. The sequence runs continually and looks like two short flashes of the LED.

Table 3-1 shows the possible GAP board status LED flash sequences. Also see Illustration L4748A for LED locations on the GAP board.

TABLE 3-1
GAP BOARD STATUS LED FLASH SEQUENCES

LED Name	State	Flash Sequence
DS2 (Heartbeat LED)	System is OK	Single flash On/Single flash Off with a period of 5 seconds and a 50% duty cycle.
DS2 (Heartbeat LED)	Boot code DUART Test Failure	Single flash On/Single flash Off, 50% duty cycle
DS2 (Heartbeat LED)	Boot code External Static RAM Test Failure	Double flash On/Single flash Off, 50% duty cycle.
DS2 (Heartbeat LED)	Power-up Interrupt Test Failure	Triple flash On/Single flash Off, 50% duty cycle.
DS1	+5V Indicator	When lit, this indicates that +5V is present. If it is not lit, +5V is not getting to the GAP.



GAP BOARD STATUS LEDS
ILLUSTRATION L4748A

4- MASTER INTERFACE (MIF) BOARD THEORY

Description - This material describes the master interface (MIF) board and its interconnections in Signa Horizon products.

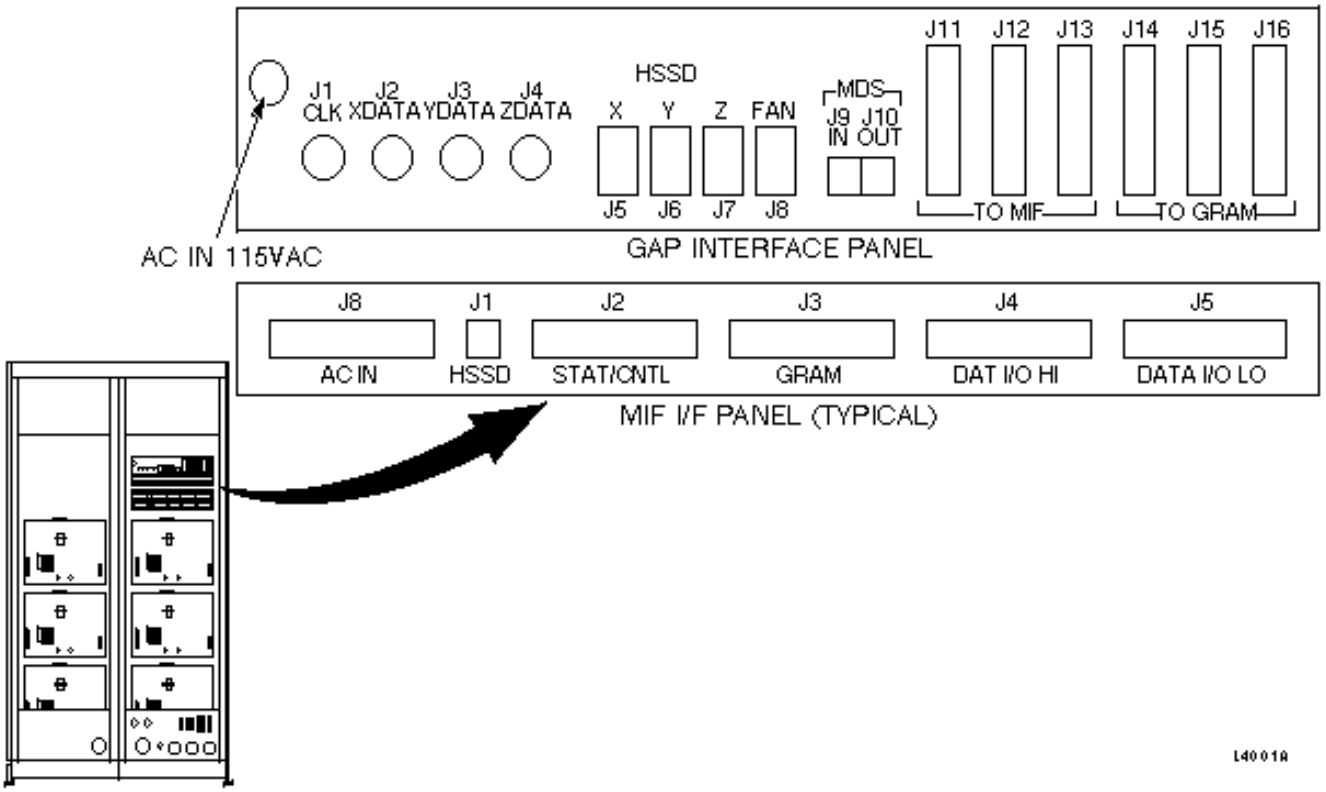
4-1- Introduction

The MIF board converts the digital waveform into an analog signal, and produces a control signal that is sent to the power modules for amplifying the waveform. It also serves as a status and control interface between the GAP board and the power modules.

4-2- Interconnections

4-2-1 MIF Module Board Rear Interface Panel

Status and control functions between the GAP board and the MIF board are transmitted through the MIF I/O line J2 (see Illustration L4001A). The high speed serial data (HSSD) signal from the GAP board connects to the MIF board interface panel at J1.



MIF & GAP I/F PANEL INTERCONNECTIONS: DOUBLE-BAY 8645 CABINET, REAR VIEW
ILLUSTRATION L4001A

4-2-1-1 Signa Horizon

The MIF board receives the digital gradient data and gradient clock signal via fiber optics J1, J2, J3, and J4 (on the GAP interface panel) from IPG. One data set is passed on through to the MIF board. The DIP switch S4-8, on the front of the MIF I/F panel has a setting for configuring a GRAM in or out of the system. For Signa Horizon, this switch is set for configuring the GRAM out of the system. Therefore, the circuitry that passes the data on through the MIF board for conversion from digital to analog is used. The MIF incorporates a digital-to-analog converter (DAC) to convert the HSSD digital waveform signal into an analog signal. The MIF scales the analog signal according to a preset gain, and sends the resultant control signal to the power modules via J5, J6, J7, and J8.

Connections to the power modules are at J4 and J5 on the MIF interface panel.

4-2-1-2 Signa Horizon HiSpeed and Signa Horizon EchoSpeed

The MIF board receives two sets of digital gradient data and gradient clock signal via fiber optics J1, J2, J3, and J4 (on the GAP interface panel) from IPG. One data set is passed on through to the MIF board, while the other set is passed on to the GRAM. The DIP switch S4-8, on the front of the MIF I/F panel, has a setting for configuring a GRAM in or out of the system. For Signa Horizon HiSpeed and Signa Horizon EchoSpeed, this switch is set to configure the GRAM in the system; therefore, the circuitry that passes the data on to the GRAM, via a 25-pin cable is used. The GRAM then converts the signal from digital to analog. At this point, the gradient data are called *Vcontrol*. The data are then passed back to the MIF via the same 25-pin cable, and sent to the power modules.

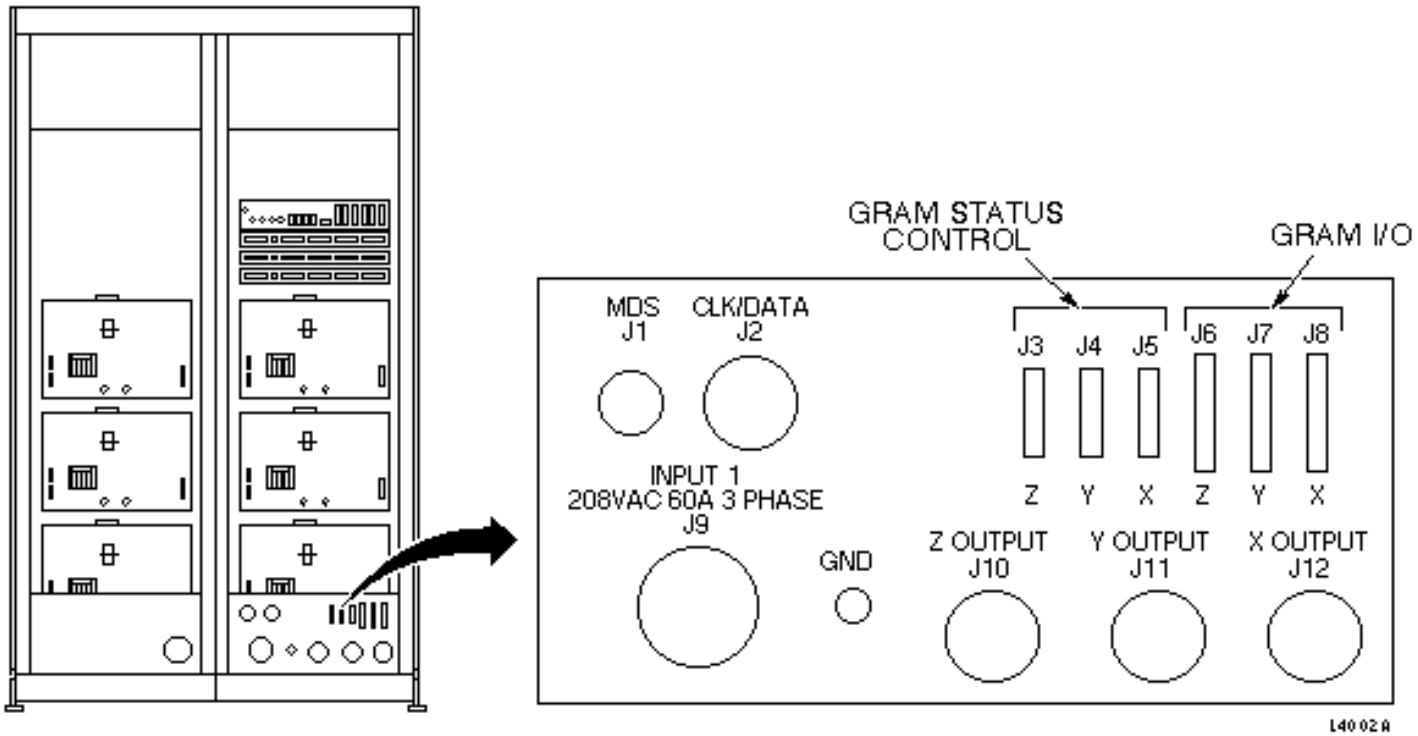
Connections to the power modules are at J4, and J5 on the MIF interface panel. Only J4 is used in the P5 (single-bay) 8645 gradient amplifier cabinet (Signa Horizon HiSpeed). The signal connection to the GRAM is at J3. The *x*, *y*, and *z* MIF boards connect to the GRAM via the gradient interface panel, ports J3, J4, and J5.

4-2-1-3 Gradient Driver Tests Special Note

If the gradient driver tests are used for Signa Horizon, Signa Horizon HiSpeed, or Signa Horizon EchoSpeed systems, the data may be routed differently, depending on in which mode the test is. For example, for Signa Horizon HiSpeed and Signa Horizon EchoSpeed, if the test is in *voltage control mode*, all data paths are consistent with the above-mentioned sections. However, if the system is a Signa Horizon HiSpeed or Signa Horizon EchoSpeed, and the gradient driver tests are run, and are in the current control mode, then the gradient data use the same path that the Signa Horizon uses, completely bypassing the GRAM.

4-2-2 Gradient Interface Panel

The *x*, *y*, and *z* MIF boards connect to the GRAM via the gradient interface panel ports J3, J4 and J5 (see Illustration L4002A).



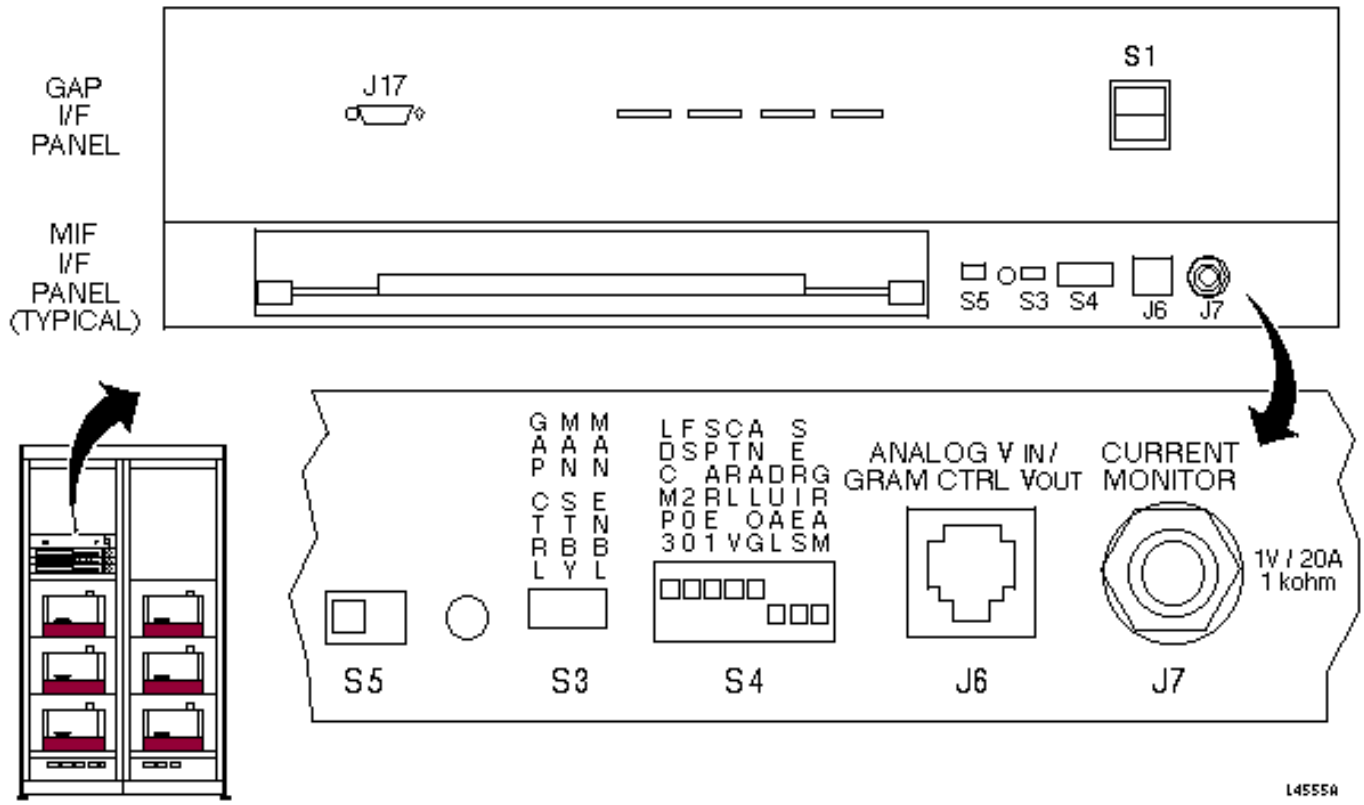
I/F PANEL, P4 CONFIGURATION: 8645 GRADIENT CABINET, REAR VIEW
ILLUSTRATION L4002A

4-2-3 MIF Module Front Interface Panel

Illustration L4555A (see Section 4-2-3) shows the ANALOG V_{IN}/GRAM CTRL V_{OUT} connector on the MIF module front panel. This connection has two functions:

1. Service personnel can monitor the voltage signal from the GRAM.

2. When the GRAM is not connected, it can be used as an optional input for analog signals (if the MIF board is in analog input mode instead of the normal digital input mode). The MIF can use the analog input from ANALOG V_{IN} instead of the analog voltage from the DAC input. This will not be used for product.



MIF FRONT PANEL DISPLAY
ILLUSTRATION L4555A

The front panel current monitor allows service personnel to monitor the current through the shunt resistor and, hence, the gradient coil.

4-3- MIF Module Front Panel Switch Settings

S4 on the front panel of the MIF module is configurable for the type of system that is installed. Positions 1, 2, 3, 4, and 5 are usually all in the off position. Position 1 is for load compensation; position 2 is for full scale of 200 amps; position 3 is a spare, and is not used; position 4 is control voltage, and position 5 is analog.

Positions 6, 7, and 8 are for dual power modules per axis, series connection of power modules, and GRAM present, respectively. These switches are the only ones used to configure the system for this release. Refer to Illustration L4555A in Section 4-2-3 and table 4-1.

TABLE 4-1
MIF SWITCH 4 SETTINGS

Switch number	1	2	3	4	5	6	7	8
Signa Horizon Product Configuration	off	off	off	off	off	on	on	off
Signa Horizon HiSpeed Product Configuration	off	off	off	off	off	off	on	on
Signa Horizon EchoSpeed Product Configuration	off	off	off	off	off	on	on	on

SPI checks the `MRconfig.cfg` file to compare the software configuration of J6 through J8 with the hardware settings of these switches. If the switches differ from the `MRconfig.cfg` file, SPI logs an error, and does not allow the gradient driver subsystem to go to the ready mode.

5- ASM/GASM THEORY

Description - This document describes the analog service module (ASM), the GRAM analog service module (GASM), and their function in Signa Horizon products.

5-1- Introduction

The ASM and the GASM are service tools designed to provide signal monitoring during system operation, and diagnostic information regarding the gradient driver closed loop analog circuit during the gradient driver tests.

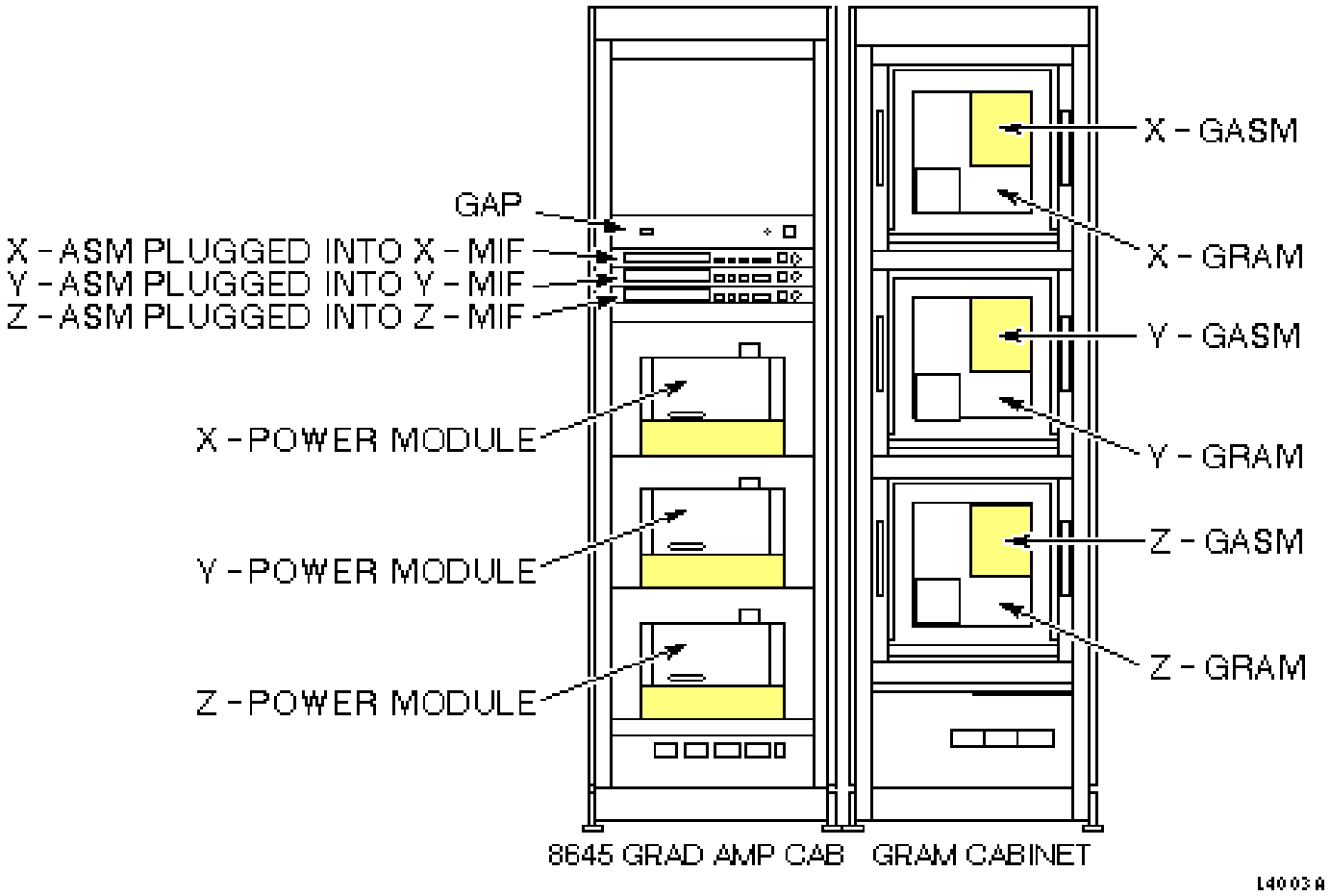
The ASM provides performance information of the power modules within the 8645 gradient amplifier cabinet. The GASM provides performance information of the GRAMs within the GRAM cabinet. They provide digitized values of the voltage, current, and temperature of a module. These sampled signals are monitored by the GAP application software. Any signal, that is out of specification is recorded, and an error is reported to the message log.

A software diagnostic tool has been created to test the gradient driver subsystem by using the ASM and GASM (if present). This diagnostic tool is a hybrid digital and analog diagnostic test. See the procedure for Gradient Driver Tests for additional information relating to the gradient driver tests. Power-up tests are detailed in the procedure for Gradient Driver Power-Up Diagnostics.

5-2- System Compatibility

The ASM boards are interchangeable between axes within an 8645 gradient amplifier cabinet, and between systems without field adjustment. In addition, GASM boards are interchangeable between axes within a GRAM cabinet, and between systems, without field adjustment.

The ASM plugs directly into the master interface (MIF) board within the MIF module contained in the 8645 gradient amplifier cabinet. There is one MIF per axis and one ASM per axis (see Illustration L4003A).



8645 GRADIENT AMP CABINET, SINGLE-BAY (P5) & GRAM CABINET: FRONT VIEW
ILLUSTRATION L4003A

The GASM is a plug-in board that connects to the GRAM control board. There is a GASM for each axis (see Illustration L4003A above).

5-3- Functional Requirements

5-3-1 ASM Signals

The ASM monitors various functions inside the 8645. It transmits information to the GAP board whenever the GAP application polls the ASM. Software determines how often this occurs. The ASM is controlled by GAP through the MIF. The ASM monitors a number of voltage, current, and temperature variables:

- Temperature signals from four sensors in the positive and negative current wells of the high and low power modules.
- Temperature signals from sensors in the 3-phase toroid transformers of the high and low power modules.
- Output current of the high and low power modules.

- Total output current. If the power modules are connected in parallel, the individual currents are summed by the MIF. If the power modules are connected in series, the current is sampled from the high power module.

- Output voltage of the high and low power modules.

- Output voltage from the MIF to the power modules.

- DAC voltage in the MIF. The DAC converts the digital input from the GAP HSSD connection to an analog signal. The analog voltage is sampled for use as a control signal, to compare with the voltage across the power module shunt resistor, and to produce the error signal. If the MIF is in analog mode, the ASM reads the input from the ANALOG V_{IN}/-GRAM CTRL V_{OUT} connector instead of the DAC voltage.

- DAC error signal. This is the difference between what the power module current should be, and what it actually is. It is a monitoring function only; no correction occurs.

- ASM board precision voltage. This 1.235V source is used as a reference value to adjust other values if necessary.

- Calibration status. A register records whether the ASM is properly calibrated with the MIF board.

These signal names are provided for identification because they will appear in the error log. The power module and ASM block diagram identify where the signals exist. (This block diagram is still under development.) The signals that are monitored by the ASM are:

Iout–H/L: Power module high/low current output

PXTemp–H/L: Power module high/low positive transistor temperature

Vcc–H/L: Vcc levels for the high and low power modules

NXTemp–H/L: Power module high/low negative transistor temperature

VMIF: MIF control voltage

Vout–H/L: Power module high/low voltage output

XFTemp–H/L: Power module high/low transformer temperature

+5digref: +5V digital used by A/D converter (divided by 4 to get 1.235V)

15REF: 15REF as a virtual ground

VDAC: Voltage of the output of the HSSD D/A converter before the scaling

5REF: 5REF as a virtual ground

VDAC_del: Scaled VDAC signal that has been passed through a fixed two-pole low-pass filter adjusted to zero offset and gain

1.235V: Reference used to calibrate the gain of A/D converter

VDAC_err: Created by subtracting VDAC_del from ITOT and gaining the result

AGND: Analog ground

5-3-2 GASM Signals

These signal names are provided for identification because they will appear in the error log.

IREG: Integrated current error

VFILT: GRAM output voltage

VBUS1: Bus voltage 1

VCTRL: Control voltage for Techrons

TRI0: Triangular reference waveform for PWM 0 degree phase shift

VBUS2: Bus voltage 2

ASPR0: Analog spare 0

VIN: DAC Ldi/dt to command the GRAM PWM voltage

LINT: Integrator output for test signal

VBUS3: Bus voltage 3

VBUS4: Bus voltage 4

VREGF: Output of voltage regulator

IERROR: GRAM current error signal

ASPR1: Analog spare 1

+5digref: +5V digital used by A/D converter (divided by 4 to get 1.235V)

15REF: 15REF as a virtual ground

IGRAD: Voltage of the output of the HSSD D/A converter on the GRAM.

VBUSA: Average of four bus voltage.

5REF: 5REF as a virtual ground

IGRAD_del: Scaled inverted IGRAD signal that has been passed through a fixed one-pole low pass filter, and has had gain and offset adjusted

1.235V: Reference used to calibrate the gain of A/D converter

ICOIL: Current detected through the coil

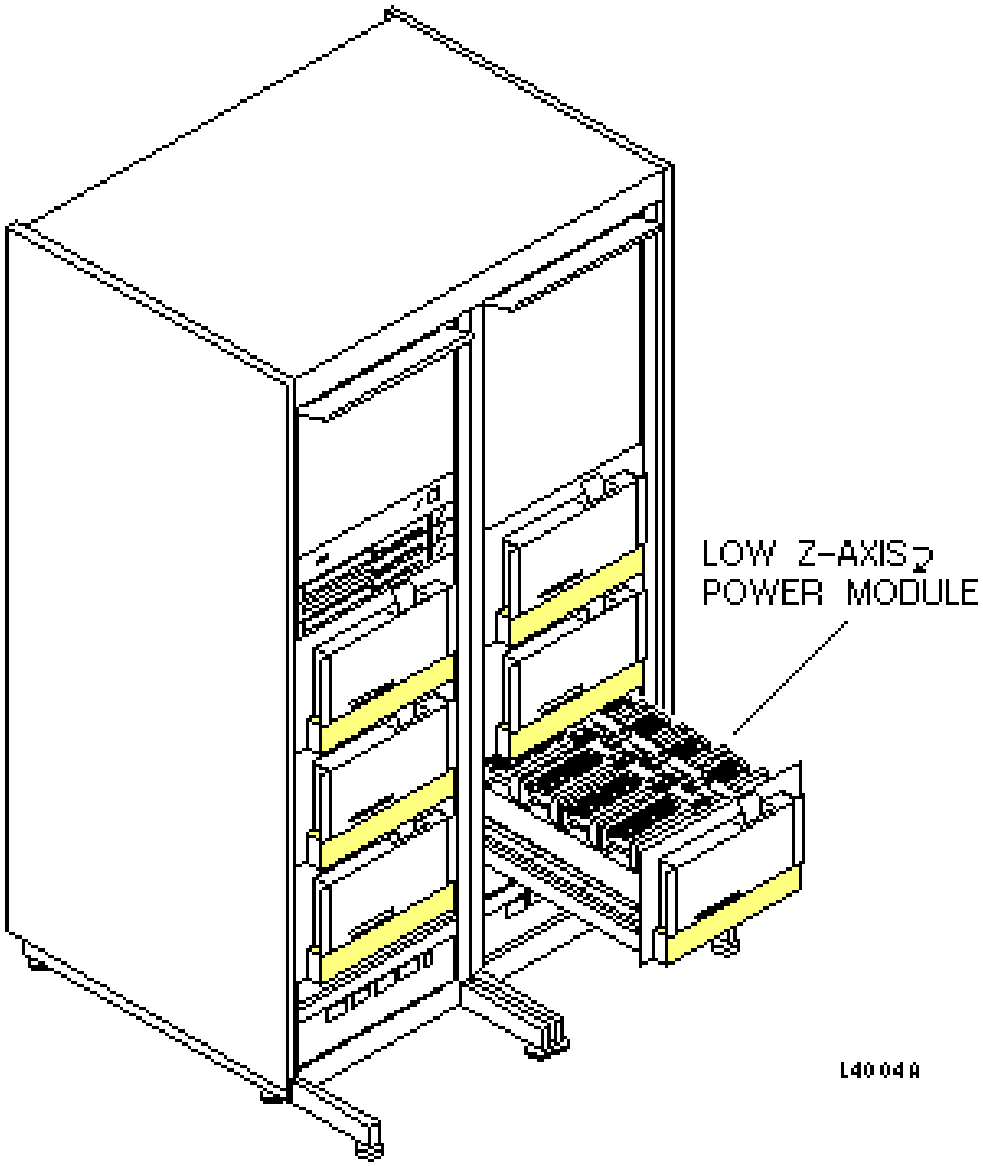
IGRAD_err: Created by subtracting IGRAD_del from the ICOIL and gaining the result

6- POWER MODULE THEORY

Description - This material discusses the theory of power module operation.

6-1- Introduction

Power modules transfer energy in a controlled manner from an available supply to a load. The energy comes from a 208Vac line converted to a dc voltage by a toroid power supply and polyphase buck module (PPBM). In correspondence to an input signal, the main board and output stages modulate the output voltage and current. The load is the epoxy-filled gradient coil, or the GRAM in series with the epoxy-filled gradient coil (see Illustration L4004A).

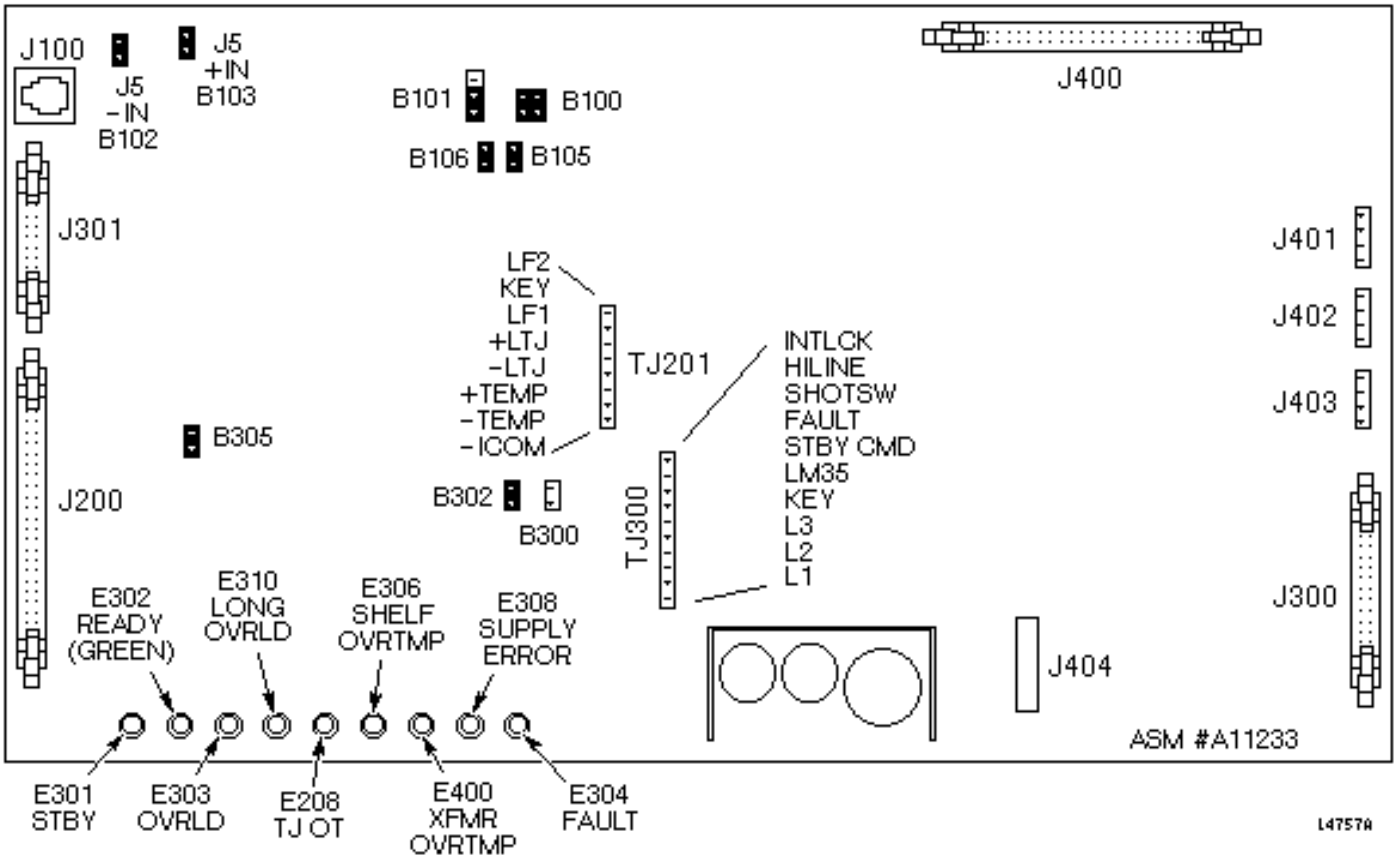


8645 DOUBLE-BAY (P4) GRADIENT AMPLIFIER CABINET
ILLUSTRATION L4004A

6-2- Main Board

The main board provides the signal interface, protection, status, control, and interlock circuits for the power module. The board interacts with the other sections, other power modules, and the master interface (MIF) board.

Main board connections (see Illustration L4757A) go to the MIF J200, the interconnect board J400, interlock ports J 300, and the PPBM J501. For test purposes, a modular analog input connector J100 is also available.



8645 MAIN BOARD
Illustration L4757A

6-2-1 Interface

The main board receives signal input from the MIF. It monitors power module status, and transmits information of various voltage, current, temperature, and error conditions to the MIF and the ASM.

6-2-2 Output Control

The main board provides the voltage control loop for the output stages. The last voltage amplifier stage drives the predriver boards of the output stages.

The current monitor on the main board measures the voltage across the shunt resistor, between common and sampled common. The voltage at the output of the current monitor is proportional to the current flowing through the shunt resistor.

The error amplifier compares the input signal and output. The difference in the waveforms of input and output is the error signal. The error amplifier amplifies the error signal to make the power module compensate and track the input waveform.

6-2-3 Protection Circuitry

Protection circuitry prevents damage to the power module components due to excessive heat, current, or voltage.

A thermocouple in the middle toroid transformer sends temperature proportional signals to the main board. When the temperature is too high (170º C) the circuit shuts off the power module.

On the high side heat sinks, switches rated for 130º C protect the unit from overheating. On the low side, heat sink thermal sensors send a temperature proportional signal to the transistor junction temperature simulation circuitry on the main board.

Power transistors are difficult to protect. The junction, or *die*, temperature is a leading cause of transistor failure, but it is impractical to measure the temperature directly; therefore, an indirect approach must be used. Temperatures can be simulated electronically by using a resistor capacitor network with an electrical response that matches the thermal response of the power transistors. The thermal sensors in the low side heat sinks provide baseline temperature information, and calculations based on voltage and current through the output transistors provide an approximate temperature value inside the transistor. If the protection circuit determines the junction temperature to be above 200º C, it temporarily reduces current to the output stages.

The fault detection circuitry detects a short circuit across the Vcc power supply. Normal current flow is through one high side quadrant, through the load, and through the opposite low side quadrant. If both high side or low side quadrants are conducting at the same time, the load is bypassed and a short circuit develops across the Vcc power supply. The fault circuit shuts off voltage supplied to the output stages, and remains in this state until power is reset.

6-2-4 Status Indicators

LEDs on the front panel of the main board report its condition with status indicators. See table 6-1.

TABLE 6-1
MAIN BOARD STATUS INDICATORS

Status	LED Indicator	Function
READY	Green	The power module is in normal operational mode.
OVERLOAD	Yellow	For longer than 0.05 milliseconds the output waveform did not match the input waveform. The light remains on as long as the overload condition exists.
LONG	Yellow	For longer than 35 milliseconds the output waveform did not match the input

OVERLOAD		waveform. The light remains on as long as the overload condition exists. The circuit breaker must be cycled, turned off, and back on, to reset the power module.
TRANSISTOR OVERTEMP	Yellow	The output transistor junctions were determined to be too hot. Current in the output stages is reduced until the temperature returns to a safe level.
TRANSISTOR FAULT	Yellow	A short circuit was detected in the output stage transistors. The power module was latched in Standby. The circuit breaker must be cycled, turned off and back on, to reset the power module.

6-2-5 Interlock

Interlocking allows multiple power modules to power a common load. In each of the three axes of the 8645 P4 configuration, wiring two power modules in series doubles the maximum voltage to the load.

When two modules are linked in series, one becomes the *high power module*, providing the positive reference output. Its output voltage is in phase with the input signal. The other becomes the *low power module*, providing the negative reference output. Its output voltage is out of phase with the input voltage. The sum of the two outputs flows through the load.

Joining two power modules means that both must operate synchronously. Both must be either on or off at the same time. If one were to enter the standby mode while the second was putting out current, the current flowing through the first amplifier could damage it.

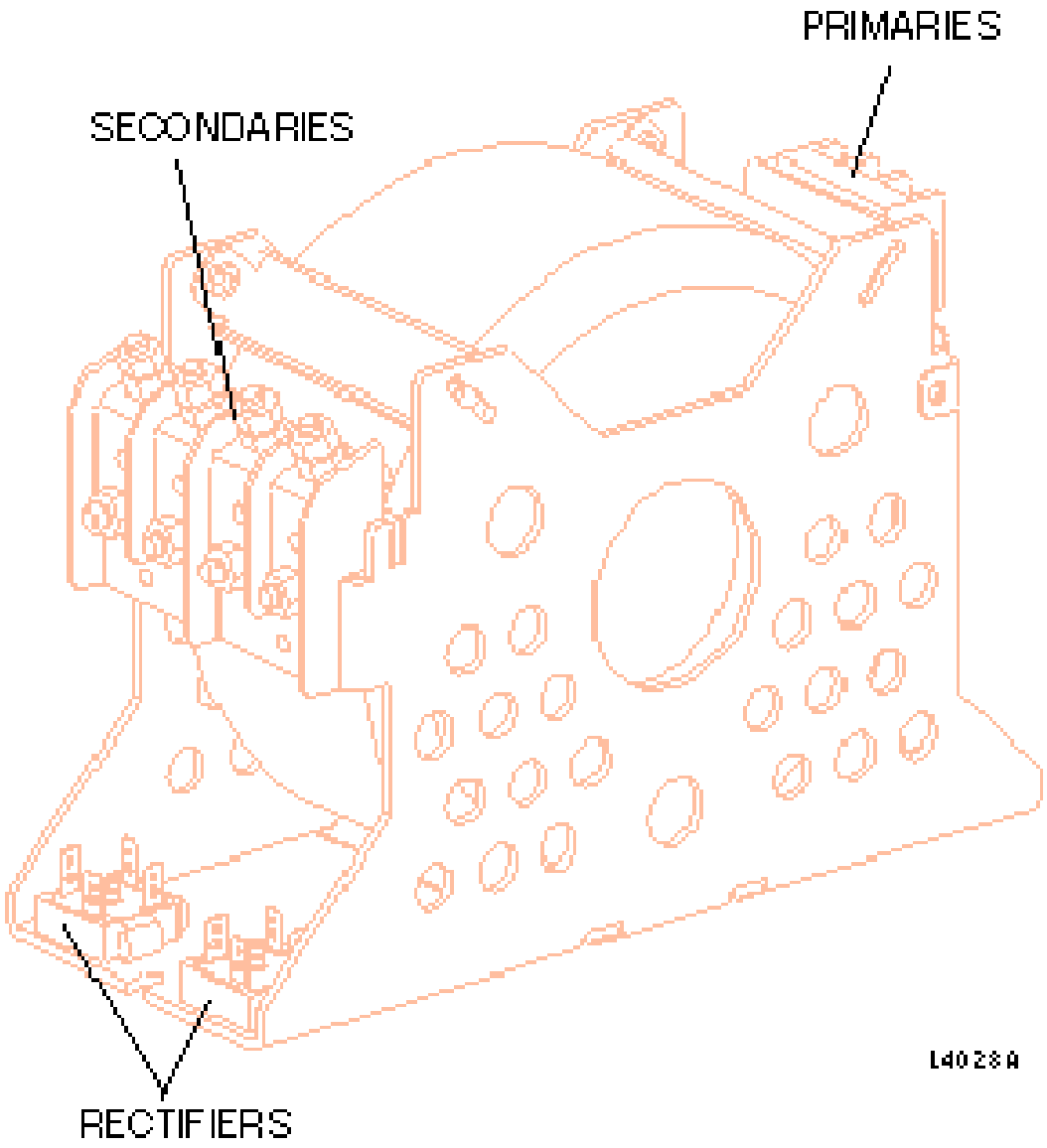
If one module shuts down, the main control board puts the other module into standby mode. When the first power module is enabled again, the other module is checked to see if it is operational before both amplifiers are put into the ready mode.

The interlocks are optically isolated and daisy-chained, thus, more modules can be added as needed.

6-3- Toroid Power Supply

The toroid power supply, also known as the *bulk dc power supply*, converts 3-phase 208Vac to 200Vdc (nominal) at up to 200A peak, or 140A RMS. Three toroidal power transformers tap each of the three ac power lines (phases A, B and C) in a wye configuration. The transformers are protected by a 50-amp 3-phase breaker between the power supply and the ac line.

Toroidal transformers are used because they are smaller and lighter than conventional laminated transformers having the same power ratings in this application. Since their magnetic flux is confined to the circular core material, they are more efficient and generate smaller stray magnetic fields than do transformers constructed with other geometries. See Illustration L4028A.



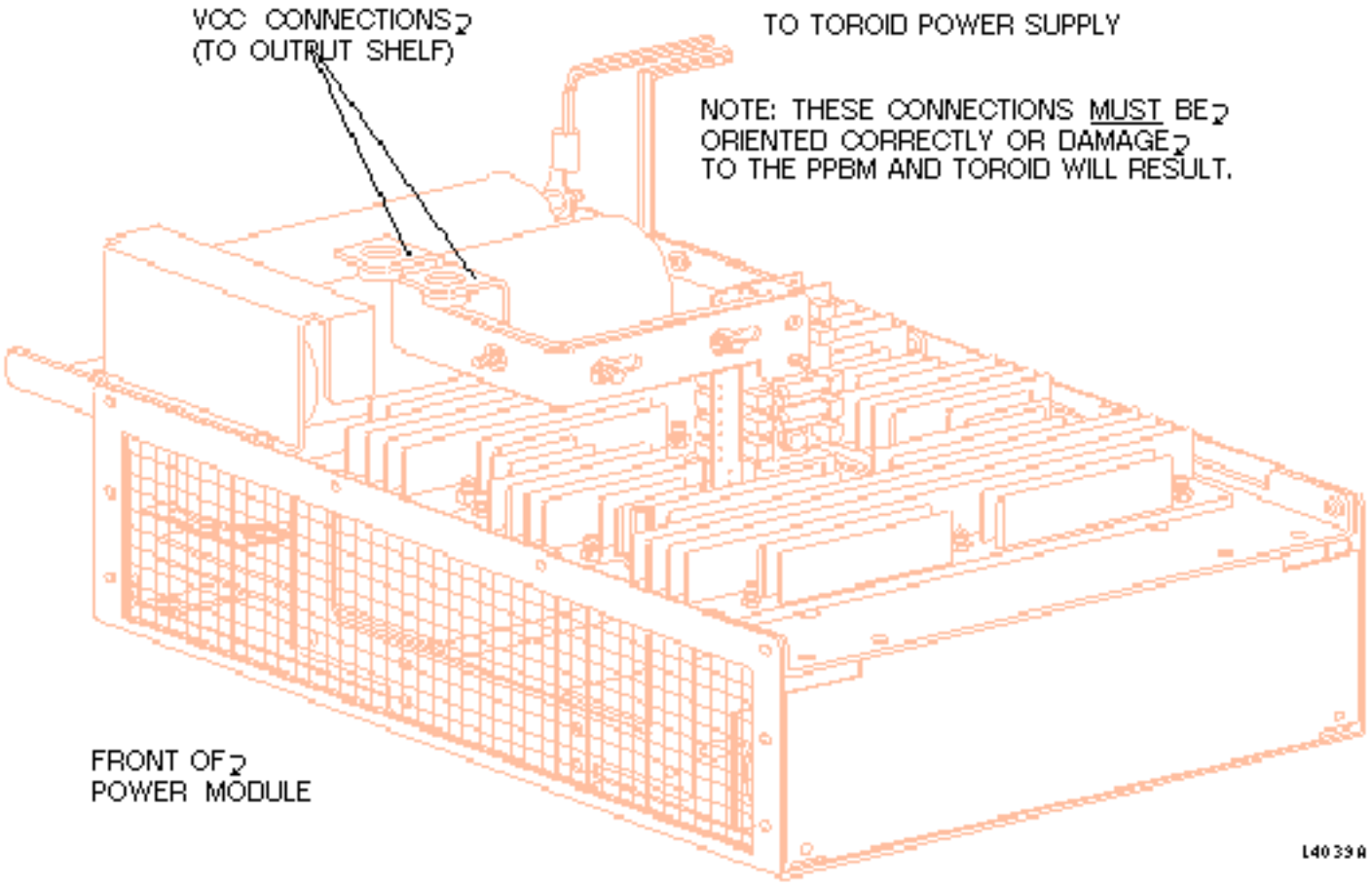
POWER MODULE TOROID POWER SUPPLY
ILLUSTRATION L4028A

Each transformer has two secondary windings. One is connected in a wye configuration with one secondary in each of the other transformers. The other secondary is connected in a delta configuration. The windings lead to six rectifier assemblies joined in parallel to a common output. The wye-delta configuration yields maximum ripple frequency, minimum ripple voltage, and maximum power factor. The rectified 200Vdc output powers the PPBM.

A fourth, smaller toroidal transformer on phases A and C, supplies 38Vac center-tapped and 9Vac to the power supply circuit on the main board. On the main board the ac voltages are converted to regulated ±15Vdc, ±5Vdc, and unregulated ±24Vdc.

6-4- Polyphase Buck Module

The PPBM supplies wide-ranging voltages, between 10 and 180Vdc, as needed to the linear, bridged power amplifier (see Illustration L4039A).



POLY PHASE BUCK MODULE
ILLUSTRATION L4039A

In a linear amplifier, the output devices act as series regulators. The devices dissipate the power difference between what is available from the power supply, and what is demanded by the load. Power dissipation is a product of voltage across and current through a component. Power dissipation over time causes energy dissipation or heat. Excess heat dissipation in semiconductors degrades product reliability and efficiency. Heat dissipation must be kept as low as possible in the output devices, while still supporting the required load currents. Such a design causes lower energy dissipation in the output devices, improved efficiency, and higher reliability.

The PPBM maintains voltage as low as is practical, typically 5 volts, across the output devices of any conducting quadrant. The total PPBM voltage, Vcc, is slightly higher than the final output voltage of the power module.

The PPBM is a switch-mode, pulse-width modulated (PWM) dc/dc regulator. The module functions as a high-power-quick-response power supply. Because the needed output voltages can change rapidly, up to 40 volts per microsecond, the PPBM must also be able to respond quickly.

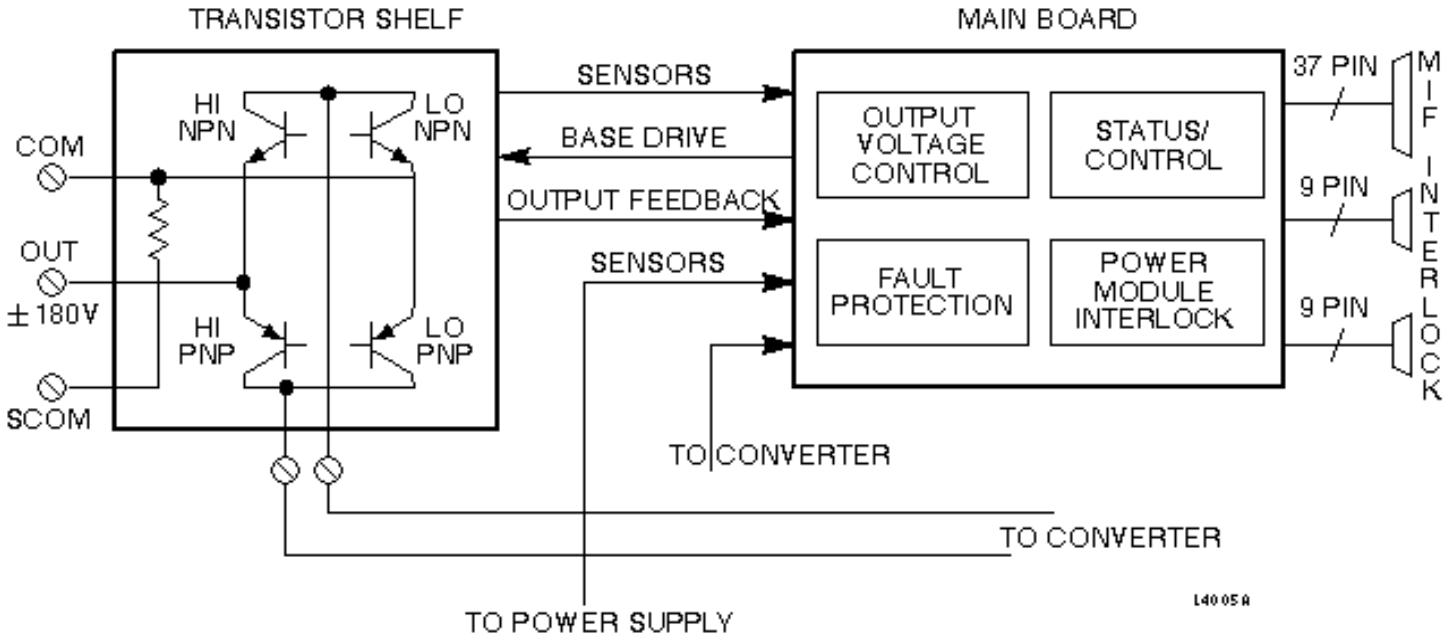
The PPBM consists of eight time-interleaved PWM buck converters. In each buck converter, the voltage output is regulated by the length of time the series power transistors are on. The output voltage is linearly proportional to the input voltage and switch-on time. Longer pulse lengths produce higher voltages passing through to the output.

When the power transistors turn off, they are protected from inductive kickback by free-wheeling diodes. The diodes bypass induced current from inductors that could damage the transistors.

The converters are regulated by reference signals from a polyphase PWM controller. The controller compares the output of each converter with the magnitude of the amplifier's required supply voltage and current, and it modulates the switching duty cycle, time of switch-on divided by the total period, of the individual PWM converters.

Eight individual single-phase converters produce identical waveforms 45 degrees apart in the power conversion cycle. Each parallel 25A peak PWM buck converter operates at 250 kHz, derived from the 2-MHz system clock by a divide-by-eight function. Combined, the buck converters produce an effective operating, ripple frequency of 2 MHz and peak current of 200A.

Each converter shares a common 200Vdc input power source from the toroid power supply, and joins to a common pair of output terminals that lead to the bridged, linear power amplifier (see Illustration L4005A).



8645 POWER MODULE WIRING DIAGRAM (UPPER)
ILLUSTRATION L4005A

6-5- Output Stages

The output stages comprise a linear, bridged power amplifier. The amplifier boosts the input signal from the main control board, which has received signals from the MIF, and through the bus bar terminal connections, drives the gradient coil (see Illustration L4006A).

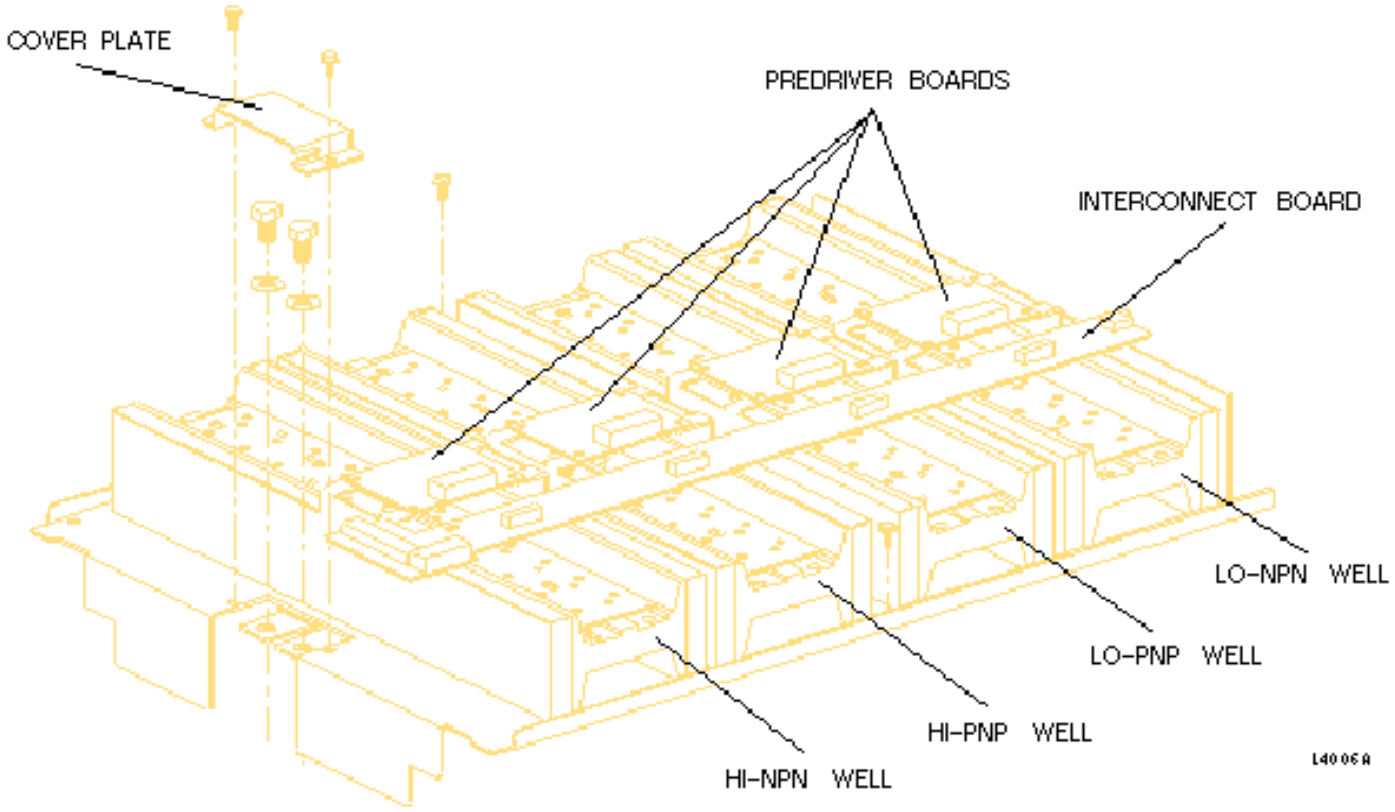


ILLUSTRATION L4006A
POWER MODULE OUTPUT SHELF

Maximum output voltage is 180 volts. Maximum current is 200 amps peak; however, total continuous power output is limited to the capacity of the power supply, approximately 10 kilowatts.

The four output quadrants, Hi-NPN, Lo-NPN, HI-PNP and LO-PNP form the bridge. The Lo sides are connected to the circuit ground and the Hi sides are connected to the output. Although each final stage consists of 20 NPN power transistors wired in parallel, the quadrants are named PNP, or NPN, because they act as if they were a single giant PNP, or NPN transistor. For positive current to flow through the load, the Hi-NPN and the LO-PNP quadrants conduct current. For negative current to flow through the load, the Hi-PNP and the LO_NPN quadrants conduct current. Each stage has two sections: the predriver board, and the output assembly.

6-5-1 Predriver Boards

The small predriver boards are mounted above each output assembly, on top of the main shelf. The shelf consists of four output stage heat sinks fastened together, plus the bus bar assembly, the shunt, and the interconnect board.

6-5-2 Output Assembly

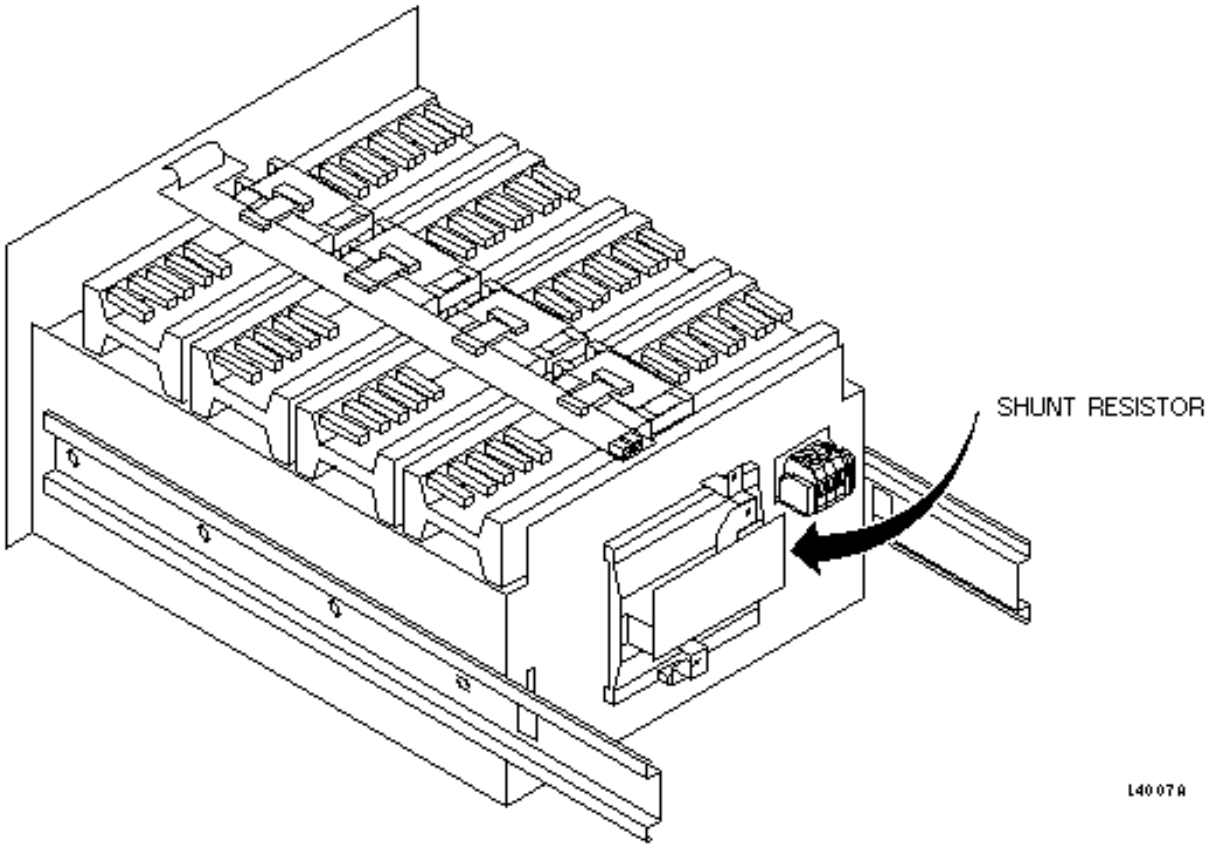
Eighty transistors are mounted on four separate electrically isolated heat sinks. Each H-shaped aluminum heat sink has air-cooled fins bonded to the vertical risers. Since the heat sinks are electrically isolated from the chassis and other output quadrants, the transistors can be connected directly to the heat sinks. This arrangement yields lower transistor junction temperatures.

Bus bars lead to the output and common terminals.

6-5-3 Current Sampling Circuit

A 5-milliohm, 250-watt shunt resistor connects the common to the sampled common terminals. In the double-bay (P4) 8645 gradient amplifier cabinet, a shunt resistor is used only on the high power module. Attaching the load between the output and the sampled common terminal allows the output current to be sampled. The voltage drop across the shunt resistor is proportional to the amount of current flowing through the load.

Sense terminals connect to the shunt resistor, as shown in Illustration L4007A. The common sense connects to the common terminal. The sampled common sense connects to the sampled common terminal. Sense wires connect to the current monitor on the main board, which in turn, sends the signal to the MIF.



SHUNT RESISTOR FOR HIGH SIDE POWER MODULES
ILLUSTRATION L4007A

6-5-4 Terminator

The output stages connect with the termination board (or terminator). The board contains a series RC circuit, providing a fixed load at all times, to aid in amplifier stability. It also provides V_{CC} filtering, augmenting the PPBM output filter.

A flyback diode assembly on the terminator prevents output voltage from exceeding the supply voltage. Inductive discharge from the load can produce extra voltage that could damage power module components. Any such excess voltage is diverted to V_{CC}.

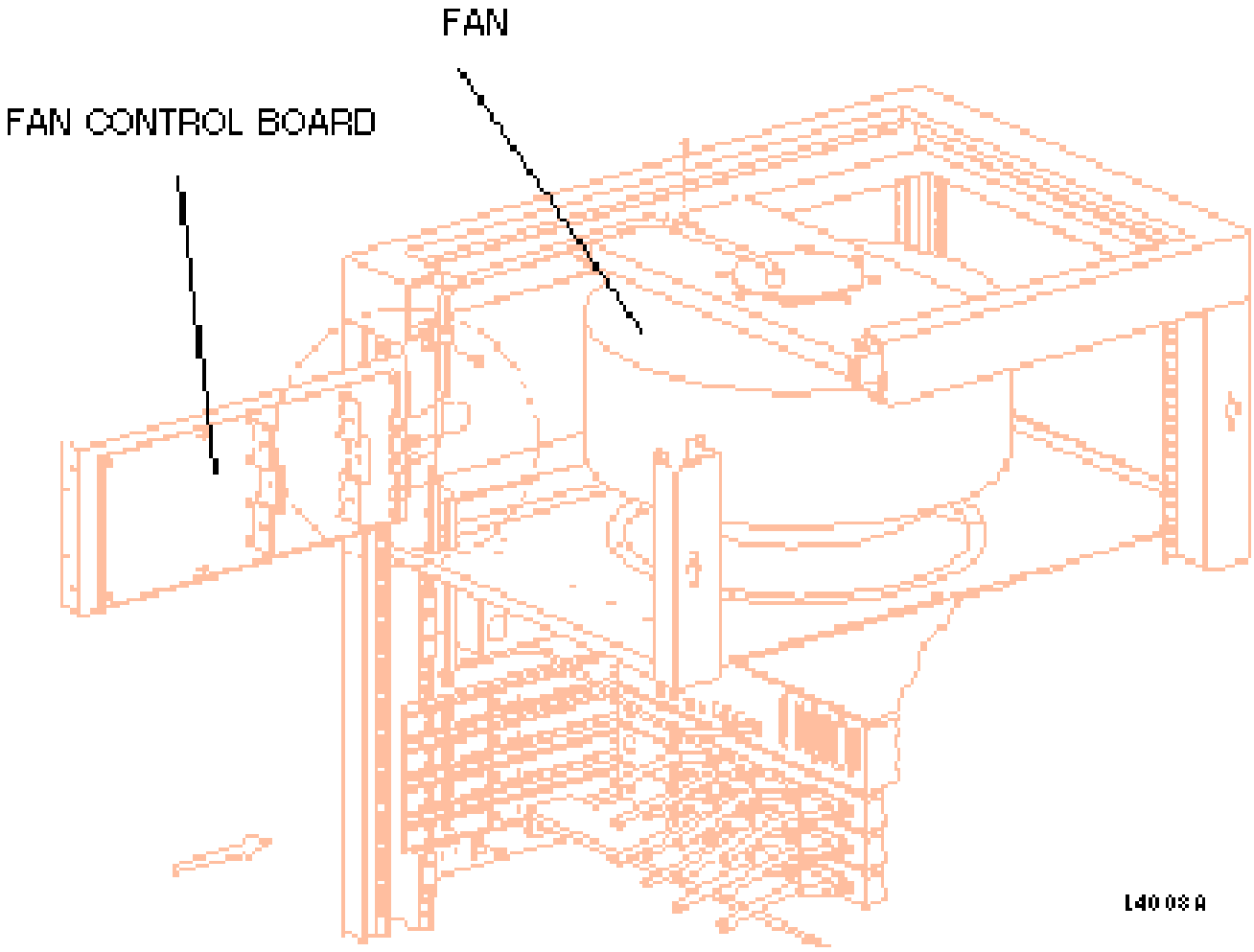
The termination board is connected to the bottom side of the output shelf. This board is not a separate FRU, but is shipped as a part of the output shelf. It can be replaced by ordering an output shelf.

6-5-5 Output Terminals

Finally, the bus bars have terminals J1-1, J1-2, J1-3 on the back of the power module for connecting a cable to the output terminal strip TS-3. A cable attached to the output terminal strip leads to the gradient coil or GRAM and gradient coil.

6-6- Cooling System

The 8645 generates a large amount of heat and requires an active cooling system. A 208Vac motor with an impeller blade provides the cooling. The fan draws cool air from the front, pulls it through the power modules, and expels the warmed air out the top. The fan assembly is shown in Illustration L4008A.



FAN ASSEMBLY
ILLUSTRATION L4008A

As long as the fan circuit breaker is on, the fan runs continuously. The fan controller regulates both fan speeds. The fan controller is, in turn, commanded by the GAP. It determines whether to run the fan at high or low speed. Typically, the fan runs at high speed during operation, and low speed during standby. This activity is software dependent.

The fan is constantly evacuating air from the cabinet, thus, air pressure is lower inside the cabinet than outside. Since this is a closed, negative pressure ventilation system, the doors on the 8645 **must remain closed**. Leaving them open stops air from properly flowing through the power modules, causing the modules to overheat.

7- GRAM THEORY

Description - This material discusses the theory of operation of the Gradient Ramp Accelerator Module (GRAM) as it relates to Signa Horizon products.

7-1- Introduction

Delivering large amounts of power to the gradient coil is difficult to accomplish in a cost-effective manner. Gradient amplifiers are expensive, and the number required to do new applications such as echo planar imaging (EPI) is cost prohibitive.

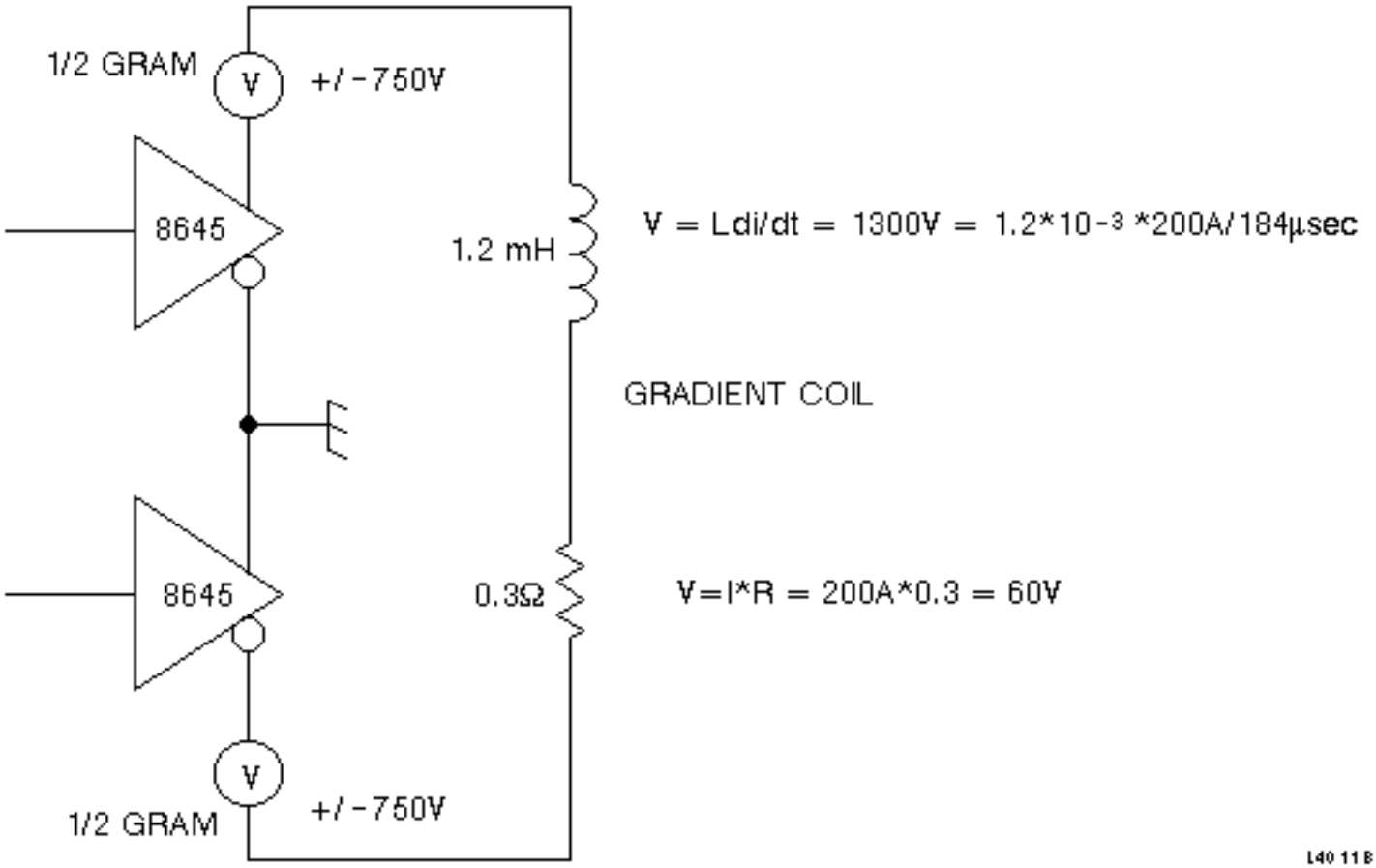
Early approaches to solving the power problem used a resonant approach. In this method, the inductance of the gradient coil is matched with a capacitor to create a resonance at a useful frequency, such as 1 kHz. Since the energy is passed back and forth between the capacitor and coil, and is not dissipated, higher peak currents can be reached than could be done otherwise. The gradient amplifier must supply only enough energy to take care of losses in this circuit. While this is an efficient use of energy, it restricts operation.

The function of the GRAM is to apply high voltage to the gradient coil during a ramp, thereby reducing ramp time significantly. When the ramp reaches a plateau, the GRAM ceases to apply voltage, and the gradient amplifier maintains the constant current flowing through the gradient coil. On the descent from the plateau, the energy from the coil is recovered in large capacitors inside the GRAM, and is stored for the next ramp.

7-2- Principle of Operation

7-2-1 Signa Horizon

High-speed imaging requires a much faster ramp speed and greater gradient strength. The GRAM provides the additional voltage required for the faster ramps, and for a new generation of linear amplifiers. The 8645 gradient amplifier cabinet is designed to provide the 2.2 G/cm required for some high-speed imaging techniques. The GRAM can be thought of as a programmable voltage source, or amplifier, connected in series with the 8645 linear amplifiers. Since it is independently controllable, it becomes possible to partition the voltages between the amplifiers such that the 8645s provide only the I*R drop of the gradient coil while the GRAM is programmed to provide the Ldi/dt voltage required for the rate of rise of current requested by the PSD. Illustration L4011B shows a simplified schematic of the GRAM gradient system operating at the Signa Horizon EchoSpeed hardware configuration.

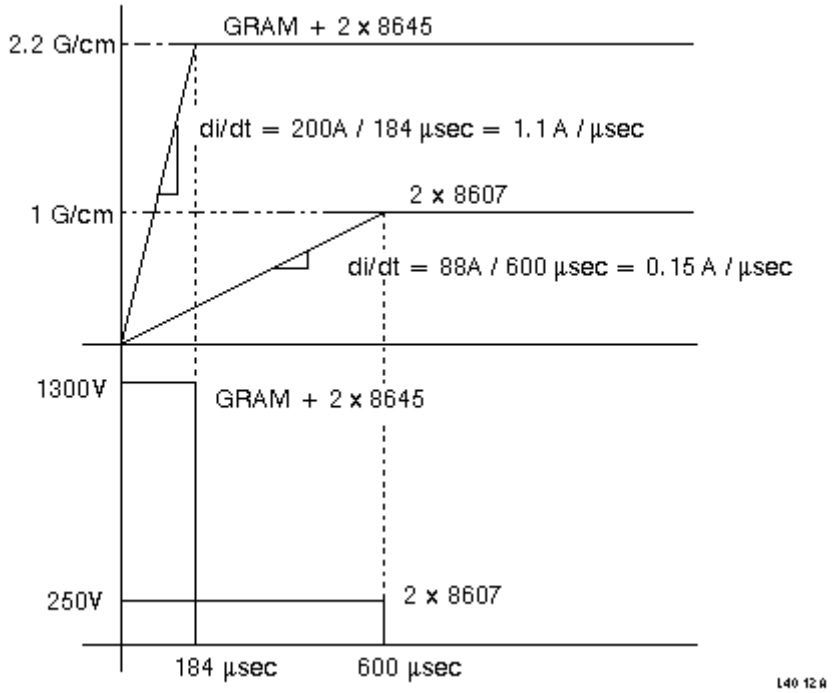


SIGNA HORIZON GRADIENT CIRCUIT
ILLUSTRATION L4011B

The GRAM assembly is part of a three-axis, high-powered gradient amplifier system for a magnetic resonance imager. Each axis consists of one or two linear amplifiers connected in series with a GRAM, and one axis of a gradient coil. The linear amplifiers and the GRAM are each separately controllable, series-connected voltage sources that are programmed to supply the IR and eddy current losses, and Ldi/dt energy required by the gradient coil. The linear amplifiers are active at all times. They supply the voltage corresponding to the I*R drop in the coil resistance, and whatever voltage is required for eddy current compensation. The GRAM is active during current ramps, and supplies the Ldi/dt voltage required to force the commanded rate of change of gradient coil current. During the flattops or plateaus of trapezoidal gradient current, Ldi/dt is zero and the GRAM operates in the freewheel mode, passing current on to the gradient coil without adding voltage to it.

7-2-2 Slew Rate Comparison

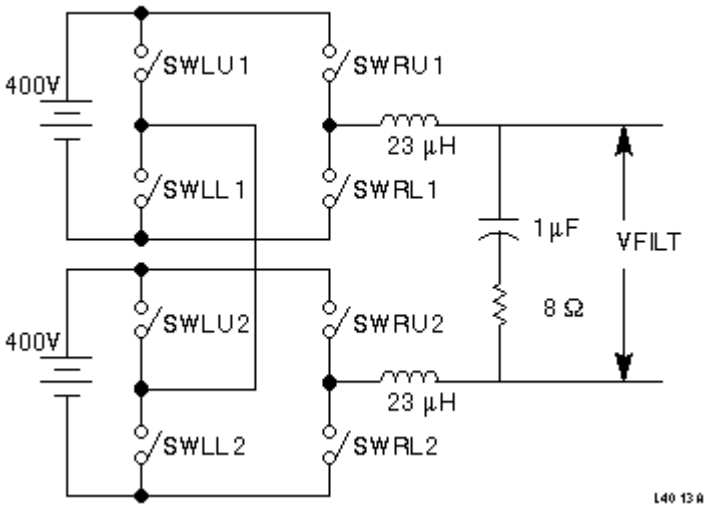
Illustration L4012A shows the relative slew rates of current of the two systems along with the voltage required to drive those slew rates. The GRAM provides about 1300 volts during the ramp to force current to 200 amps in 184 msec, while the present product can ramp only to 88 amps in 600 msec.



SLEW RATE COMPARISON OF GRAM AND TWO 8607S
ILLUSTRATION L4012A

7-2-3 Switching Amplifier Function

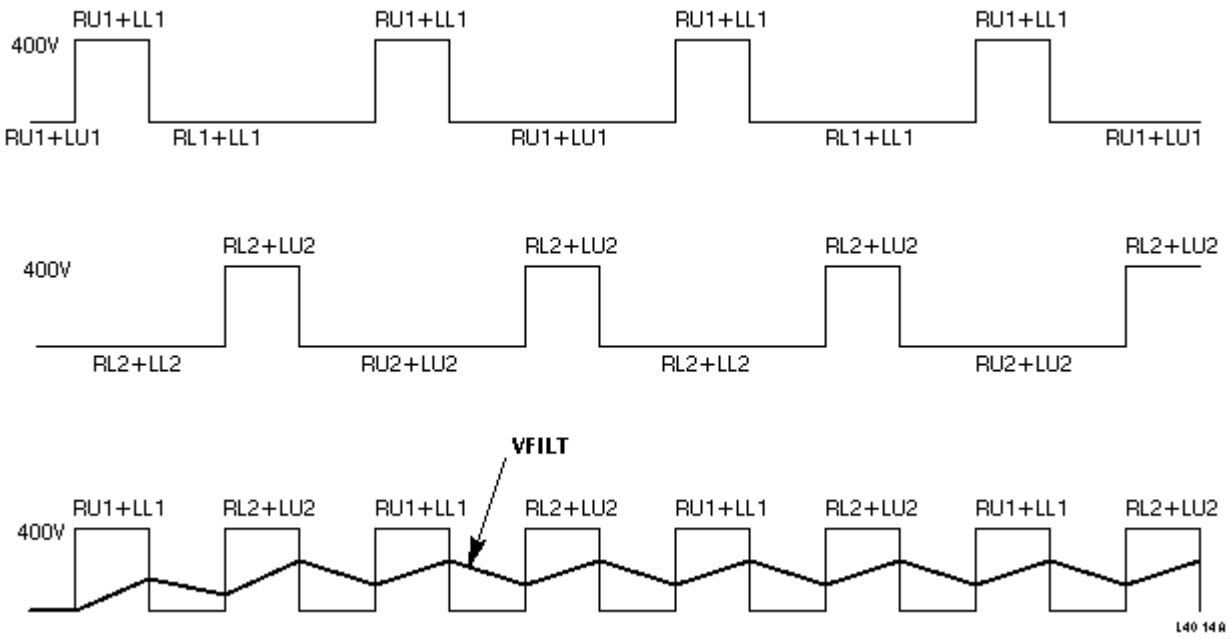
Each of the 750V voltage sources shown in Illustration L4011B (see Section 7-2-1) is actually a switching amplifier made up of two full bridge inverters connected in series, and an LRC output filter shown schematically in Illustration L4013A. The operation of each full bridge inverter can be understood by representing each IGBT as a single-pole mechanical switch with four switches connected into a full bridge circuit with a 700V battery feeding the dc bus. The inverter is capable of producing +400V and –400V, or zero volts at its output by turning the proper switches on and off. For instance, if SWRU1 and SWLL1 are closed, 400 volts is connected to its output at the midpoints of the two inverter legs. Closing SWLU1 and SWRU1 short circuits the two midpoints together producing zero volts, and closing SWLU1 and SWRL1 produces –400 volts. A second identical inverter is connected in series with the first inverter and this combination can produce five voltage states: +800V, +400V, 0V, –400V, and –800V.



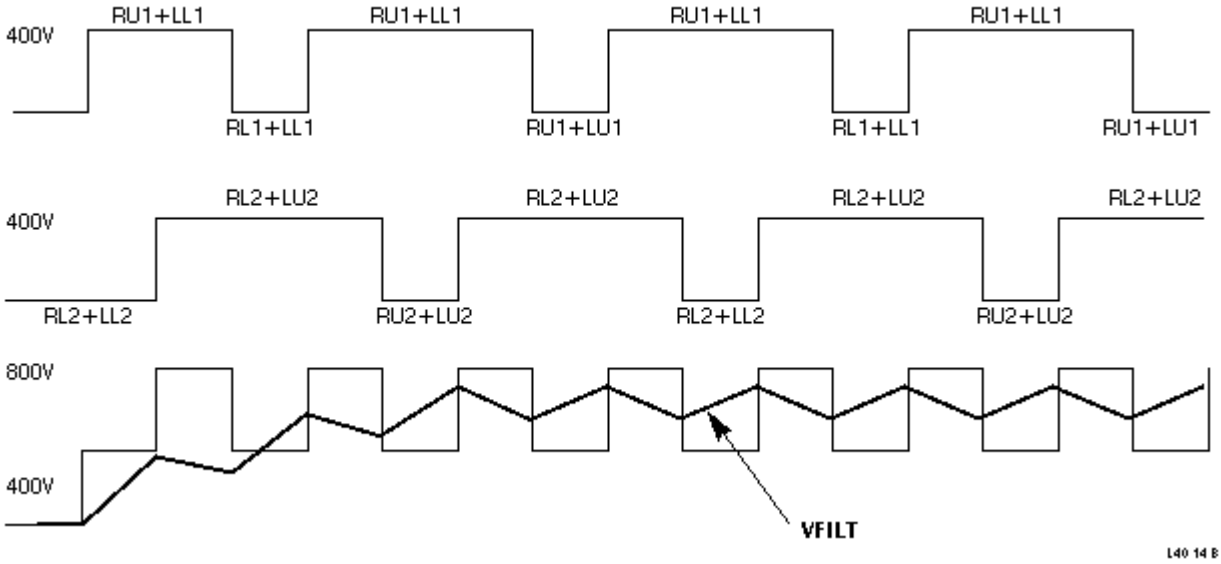
SIMPLIFIED CIRCUIT OF PULSE WIDTH MODULE AMPLIFIER
ILLUSTRATION L4013A

7-3- GRAM Control Board

Illustration L4014A and Illustration L4014B are partitioned into signal level circuits on the GRAM control board on the left, and the high-power circuits on the right. Notice the gradient coil load on the right side of the illustration. Starting at the system ground point between the two 8645 linear amplifiers, in Illustration L4014B, there is a series circuit consisting of an 8645, two series connected full bridges with an LRC output filter, a current sensor, the one axis of a gradient coil, another set of inverters with output filter, and, finally, another 8645 linear amplifier connected back to the system ground point. On the GRAM control board are the signal level electronics for two regulating loops. In the center is a current regulator that is similar to the regulator on 8607 amplifiers. It consists of a summing amplifier that compares the gradient current command from a DAC to actual coil current from a Hall-type current sensor and generates an error signal that drives the linear amplifiers in the voltage mode. At the bottom of the block diagram is a voltage regulator with a summing amplifier that compares an Ldi/dt command from a DAC with the actual voltage from the two output filters. The resultant error signal drives the pulse width modulators and gate drivers of the four full bridge inverters.



PULSE WIDTH MODULATED AMPLIFIER AT 25% VOLTAGE
ILLUSTRATION L4014A



PULSE WIDTH MODULATED AMPLIFIER AT 75% VOLTAGE
ILLUSTRATION L4014B

7-4- GRAM Power Compartment

There are four inverters with a pre-charged power supply, snubbers, and gate drivers. The dc bus for each inverter is supplied by two large electrolytic capacitors in series. These are precharged by a voltage doubler circuit driven by a 500-watt transformer at 31.25 kHz. Two discharge relays dump the capacitor energy through 20-watt resistors when the GRAM is powered down, or when it trips out.

7-4-1 Current and Voltage Sensor Circuitry

The GRAM voltage sensor board is the location of the high voltage input resistors of the differential amplifiers that monitor the GRAM output voltages. Gradient coil current is monitored by a precision dc current sensor called a *LEM* (a French acronym for a Swiss-named current sensor component) that feeds its signal to a burden resistor and amplifier on the control board.

The square-wave pulse with modulated outputs of the GRAM inverters is filtered by a coupled inductor and output capacitors with high-power damping resistors in series with each filter capacitor to damp the oscillations that occur at the transitions from current ramp to flattop. EMI filtering is provided by ferrite sleeves and bypass capacitors on the output terminals.

Both the positive and negative outputs are monitored by the two voltage sensors, and the positive output is monitored by the LEM current sensor.

7-4-2 GRAM Power Supply Board

The power supply board has two main power supplies. One is a 200-watt supply for the =/– 15V, +5V and the gate driver power, and the other one is 2-kW supply that powers the four precharged supplies for the inverter busses. A ribbon cable connects to the GRAM control board with various bus voltages and housekeeping signals.

Incoming power to the GRAM cabinet is 208Vac. It comes in from its own circuit breaker in the bottom of the GRAM cabinet and goes into an EMI filter and is rectified before application to the filter capacitors on the power supply board. The 120Vac used to drive the start-up circuit on the power supply board comes from one of the 208Vac lines to neutral.

7-4-3 Bridge Circuitry

The inverter is a full bridge formed with two insulated gate bipolar transistor (IGBT) modules. Each module contains two IGBTs connected in series, along with freewheeling diodes. Each module has a snubber board whose functions are to control switching losses in the IGBTs, and limit voltage overshoots. The left IGBT snubber board has a turn-on snubber consisting of an inductor that allows the dc bus voltage to drop during the recovery of the freewheeling diodes, limiting the energy dissipated in the IGBT. The diodes and resistors prevent the stored energy in the capacitor from dumping into the IGBT when it turns on again.

A high-frequency capacitor on the input side of the left snubber board prevents voltage overshoots due to the inductance of the wiring to the electrolytic bus capacitors. This capacitor has a current transformer in its lead that senses the current dump caused by short circuits in the inverter.

The right snubber board has turn-off snubbers like the left board and a peak charge snubber that prevents voltage overshoots locally on that board. Each IGBT has a gate driver circuit with its own electrically isolated power supply, and optically coupled on/off command. The opto-couplers for each module are connected back to back to prevent both IGBTs from conducting simultaneously, causing a short circuit on the dc bus.

A thermostat is mounted on the main heat-sink with the IGBTs. It opens at 75º C to protect the GRAM from overloads, or high ambient temperatures. All four full bridges are so equipped.

7-5- Pulse Width Modulation

Pulse width modulation (PWM) is a scheme by which the voltage is switched on and off based on the width of a switching pulse. For example, if a pulse is positive for one fourth of the time, and off three fourths of the time, the output turns on during the positive pulse, charging the capacitors, and increasing the voltage until the negative-going edge of the pulse turns off. The output then turns off. The following example illustrates how the GRAM uses two voltage sources to provide an output for the gradient driver circuit.

Illustration L4014A (Section 7-3) show a pulse width modulation waveform with filtering at 25% of maximum output voltage. Initially, both inverters are in the freewheel mode and appear as a short circuit to the output terminals. VFILT is zero and any gradient current due to activity of the 8645s flows through the inverters on switches RU1, LU1, LL2 and RL2. VFILT begins to rise when switch LU1 turns off and LL1 turns on to connect +400 volts from the bus of the first inverter to the output LRC filter.

The filter capacitor charges for 4 μsec until RU1 turns off and RL1 turns on, and then discharges for 4 μsec as the filter inductor current freewheels in the two inverters. LL2 then turns off and LU2 turns on, connecting +400 volts from the second inverter bus to the output. The filter capacitor again charges for 4 μsec, and then discharges when RL2 turns off and RU2 turns on and the current freewheels. This sequence repeats itself, and the output filter eventually reaches a steady-state average voltage of 25% with a small amount of ripple at 125 kHz.

This voltage produces a ramp of current in the gradient coil. At the end of the ramp, the control forces the inverters into a freewheel state which places a short circuit on the output filter. The oscillations of the output filter at its resonant frequency are damped by the 8Ω resistor as VFILT drops to zero. The duty cycle of the pulse width modulation is variable from 0% to 100%, giving complete control of the average voltage of the output filter. Illustration L4014B (Section 7-3) shows operation at 75% duty cycle.

It should be noted that the output frequency (62.5 kHz) of the inverter is twice the switching frequency (31.25 kHz) of each IGBT module, which is a characteristic of full bridges. Also, the two inverters are operated 90 degrees out of phase with each other so that the frequency of the sum of the two outputs is twice the inverter frequency of 125 kHz. The two pairs of inverters are operated 45 degrees out of phase, which again doubles the frequency of the ripple voltage applied to the gradient coil to 250 kHz.

The voltage of each filter circuit is monitored with a differential amplifier and the total is fed back to the filter voltage regulator, and is summed with the Ldi/dt voltage command from a DAC. The difference is the voltage error that is applied to a proportional integral derivative (PID) amplifier. This amplifier is basically an integrator that drives the inverter pulse widths to whatever value is required to force the error signal to zero at low frequency. The proportional term is a time constant in the integrator circuit that nullifies the integrator phase shift at high frequency to improve the closed loop stability, The derivative term is a differentiator on the voltage feedback signal that allows higher loop gain by anticipating overshoots of the filter voltage.

8- GRADIENT DRIVER SIGNAL OVERVIEW THEORY

Description - This material explores analog and digital signals, including their locations and interrelationships, and how they apply to Signa Horizon products.

8-1- Introduction

The gradient driver subsystem is a closed loop analog circuit. The power modules are active during the plateaus, or flat tops, of the PSD (pulse sequence data base), and the GRAM and power modules are active during ramps or transitions of the PSD. This section looks at key digital and analog signals, where the signals are located with respect to a block diagram, and how they interrelate.

The gradient driver subsystem operates in one of two modes to regulate coil current: the amplifier control mode, and the GRAM control mode.

Amplifier Control Mode: The power modules are in the ready mode. The power modules control the current. This is the normal mode when no GRAM is present.

GRAM Control Mode: The power modules and GRAM are in the ready mode. The GRAM controls the current. The power modules receive their voltage command signal from the GRAM. The combination of the GRAM and power module output voltage is used to drive current through the coil.

8-2- 8645 Gradient Amplifier Signals

Refer to table 8-1 for all signals referenced. The checkmarks in the columns indicate where the signals can be accessed to be measured.

When referencing table 8-1, remember the hardware configuration of the system that you are working on:

- Signa Horizon has two power modules per axis and no GRAM.
- Signa Horizon HiSpeed has one power module and one GRAM per axis.
- Signa Horizon EchoSpeed has two power modules and one GRAM per axis.

TABLE 8-1
GRADIENT DRIVER SUBSYSTEM SIGNAL DEFINITION

Name	Main Bd	MIF	ASM	GRAM	Signal Definition
IOUT-H	✓				IOUT High is the current flowing through the shunt on the high power module. The shunt impedance is ≅ 5 mΩ. For Signa Horizon, IOUT High measures the current flowing through the coil with the feedback signal going to the current regulation on the MIF, which is an OPAMP C-R circuit. For systems with a GRAM, Signa Horizon HiSpeed and EchoSpeed, IOUT High senses current for the IAMP overcurrent detection.
IOUT-L	✓				IOUT Low has the same circuitry as the high power module, except that there is no output shunt; therefore, the current for IOUT should be 0 amps.
ITOT-H		✓			For all product configurations, ITOT ≡ IOUT-H. ITOT is the measurement of the total current as the MIF sees it. IOUT-H is what the power module sees. ITOT is + when IOUT-H is +.
VDAC			✓	✓	For Signa Horizon, VDAC represents the command current to the MIF per axis. VDAC is on the MIF and can be measured on the ASM. For Signa Horizon HiSpeed and EchoSpeed, VDAC ∝ VCNTL that is measured on the GRAM.
VDAC_DEL			✓		VDAC_DEL is the delayed VDAC signal. The delay is approximately the type seen from the gradient amplifier current loop. It is used only when current is regulated by the power module, not by the GRAM.
VDAC_ERR			✓		This is the error signal. A comparison is made between what is expected and the predicted error (VDAC_DEL). When VDAC_DEL is subtracted from ITOT, VDAC_ERR is generated. It acts as a monitoring signal, and is used only when current is regulated by the power modules, not by the GRAM. There is a gain factor used to generate VDAC_ERR: (VDAC_DEL – ITOT) = VDAC_ERR.
VMIF-H	✓				This is the output voltage of the MIF that is transmitted to the high power module. It is the input command to the power module. VMIF is located on the MIF board, and is measured on the main board.
VMIF-L	✓				This is the output voltage of the MIF that is transmitted to the low power module. It is the input command to the power module. VMIF is located on the MIF board, and is measured on the main board.
AMP OUT-H	✓				VOUT-H is the output voltage of the high power module in response to VMIF. It is measured on the main board as AMP OUT with respect to analog ground. Power module output capabilities are ±150V AND ±200A
AMP-OUT-L	✓				VOUT-H is the output voltage of the low power module in response to VMIF. It is measured on the main board as AMP OUT with respect to analog ground. Power module output capabilities are ±150V AND ±200A. The polarity AMP OUT-L is the negative of AMP OUT-H.
±Vcc-H	✓				Vcc-H is the output voltage of the polyphase buck module in the high power module. It is measured differentially from +Vcc to – Vcc on the main board of the high power module. The range for Vcc for systems without a GRAM is 0 to ±180V. The range for Vcc for systems with a GRAM is 0 TO ±150V because the GRAM has limiter circuitry that limits the voltage from the power module.

±Vcc-L	✓				Vcc-L is the output voltage of the polyphase buck module in the low power module. It is measured differentially from +Vcc to – Vcc on the main board of the low power module. The range for Vcc for systems without a GRAM is 0 to ±180V. The range for Vcc for systems with a GRAM is 0 TO ±150V because the GRAM has limiter circuitry that limits the voltage from the power module.
+TEMP-H	✓				This is the output shelf temperature for the positive shelf in the high power module.
-TEMP-H	✓				This is the output shelf temperature for the negative shelf in the high power module.
+LTj-H	✓				This is the temperature for the transistor junction for the positive shelf in the high power module.
-LTj-H	✓				This is the temperature for the transistor junction for the negative shelf in the high power module.
+TEMP-L	✓				This is the output shelf temperature for the positive shelf in the low power module.
-TEMP-L	✓				This is the output shelf temperature for the negative shelf in the low power module.
+LTj-L	✓				This is the temperature for the transistor junction for the positive shelf in the low power module.
-LTj-L	✓				This is the temperature for the transistor junction for the negative shelf in the low power module.
XFTEMP-L1-H	✓				This is the temperature for L1 toroid in the high power module.
XFTEMP-L2-H	✓				This is the temperature for L2 toroid in the high power module.
XFTEMP-L3-H	✓				This is the temperature for L3 toroid in the high power module.
XFTEMP-L1-L	✓				This is the temperature for L1 toroid in the low power module.
XFTEMP-L2-L	✓				This is the temperature for L2 toroid in the low power module.
XFTEMP-L3-L	✓				This is the temperature for L3 toroid in the low power module
HSSD				✓	HSSD is the high-speed serial link. It is a digital bitstream with a 10-MHz clock for synchronization with the RF waveforms. It has 20 bits of resolution.
DAC_I *				✓	DAC_I is the current command, or bore flux command: the flux that is desired in the bore. Eddy current compensation must be added to this signal. This signal is sometimes also referred to as IDAC, and DACI; they are all the same signal.
IGRAD *				✓	IGRAD is the current command, DAC_I, with eddy current compensation added to it.
ICOIL *				✓	This is the actual coil current feedback from the coil from the current sensor; also called the *LEM* (a French acronym for the Swiss-named current sensor).
IERROR *				✓	DACI - ICOIL = IERROR. This is the error signal, the current that is demanded, and the actual current supplied.
IREG *				✓	ICOIL is subtracted from IGRAD. The difference is the current through a compensating network, and that current difference is IREG.
VC (Vcontrol) *				✓	IREG goes through a slew rate limiter and voltage limiter circuit. Then a gain of 2 is factored in, and the signal becomes VC. VC is the voltage command to the 8645 when the 8645 is set in voltage control mode.
Ldi/dt ∇				✓	This value is the impedance multiplied by the rate of change of current with respect to time. It is accomplished via a digital differentiator.
DAC_DI ∇				✓	The digital derivative signal Ldi/dt goes through the Ldi/dt DAC. The output of this DAC is DAC_DI. This is an analog voltage command for the GRAM. The signal is routed through the tuning

					board where there is a DAC_DI POT. This signal is also referred to as DACDI.
VFILT ∇				✓	VFILT is the actual output voltage for the GRAM module. The GRAM has a positive half and a negative half. There is a VFILT+ and a VFILT–. The two signals are summed to produce the total GRAM output voltage for this axis.
VREGF ∇				✓	VFILT is subtracted from DAC_DI and amplified through a compensating network to produce VREG. VREG is the error signal between what is the actual output of the GRAM and the voltage commanded for the GRAM. VREGF is the command to the pulse width modulators.
PWM ∇				✓	VREGF error signal becomes the pulse width modulator input and is compared with four triangle waveforms, the names of which are TRI0, TRI90, TRI45, and TRI135. The instantaneous voltage of VREGF generates the pulse width modulator waveforms. The signals are input to a series of comparators which sees the crossing of the triangle waveforms and VREGF. The outputs generate the four pulse width modulator signals, which are called +HI, +LO, –HI, and –LO. PWM is the summation of these four signals. PWM is equivalent to the unfiltered inverter output voltage applied to the coils. This signal is actually filtered when it is output to the coil.
VBUS ∇				✓	The bus voltage regulator circuitry produces four bus voltage signals. VBUS is the summation of VBUS0, VBUS1, VBUS2, and VBUS3.
VBUSREF ∇				✓	VBUSREF is 400V and is the reference voltage for VBUS.
VBUS-0 ∇				✓	This is the bus voltage for one stage of the inverters. It is associated with a series of four orange LEDs on the GRAM control board.
VBUS-1 ∇				✓	This is the bus voltage for one stage of the inverters. It is associated with a series of four orange LEDs on the GRAM control board.
VBUS-2 ∇				✓	This is the bus voltage for one stage of the inverters. It is associated with a series of four orange LEDs on the GRAM control board.
VBUS-3 ∇				✓	This is the bus voltage for one stage of the inverters. It is associated with a series of four orange LEDs on the GRAM control board.

* This symbol indicates that the signal is associated with the current path for the GRAM circuitry.

∇ This symbol indicates that the signal is associated with the voltage path for the GRAM circuitry.

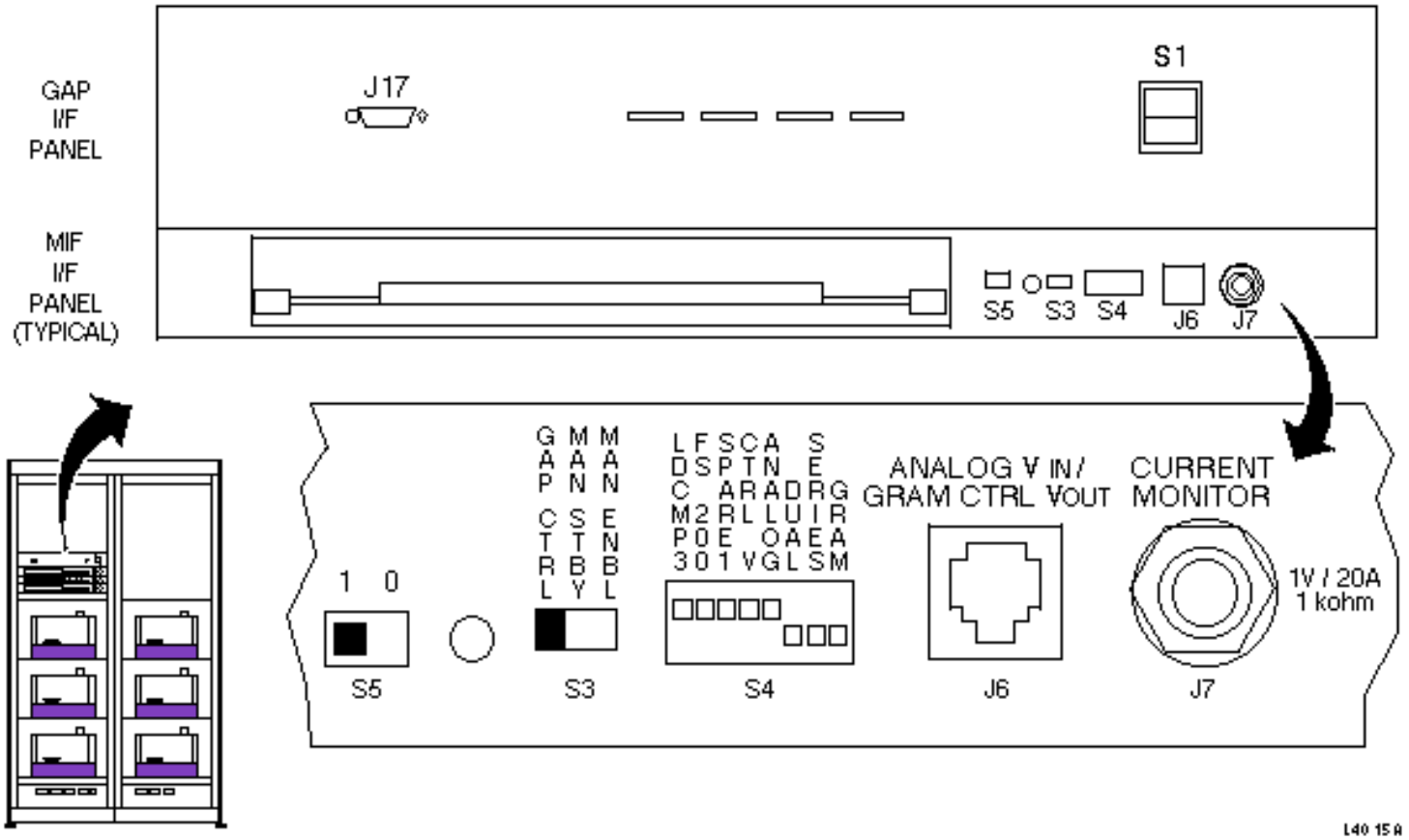
✓ This symbol indicates that the signal is measured on the board for that column.

8-3- Block Diagram Reference

Use the 8645 gradient amplifier functional block diagram as a reference for this discussion. Refer To *Direction 2153389, Signa Horizon (Release 8.x) Block Diagrams and Supplemental Schematics*, Gradient Tab, Signa Horizon (8.x) Gradient Driver Subsystem (8645 Gradient Amplifier Cabinet), Sheet 2 of 3. Table 8-1 above refers to signals that are found in these Illustrations.

8-4- Gradient Driver Modes and Controllers

There are several conditions that this flexible gradient driver subsystem can function in. From Low Side Inverter, to Current Sense Summing, to Analog Voltage In, to setting Full Scale, this subsystem can be configured in many different ways. It is important to ensure that the system is operating in product configuration. If the subsystem is configured incorrectly, the system will not function correctly, or damage can occur to the hardware. See Illustration L4015A for the configurations listed below.



FRONT PANEL FOR A MIF AND THE GAP
ILLUSTRATION L4015A

8-4-1 Low Side Inverter

When this slide switch, which is located on the MIF board, indicates Low Side Inverter, it causes the low power module to output opposite polarity signals from the high power module. This slide switch should always be in the *inverted* mode.

8-4-2 Current Sense Summing On

Current Sense Summing On is located on the MIF board. It is critical that it always be in the *off* position.

8-4-3 Analog V_{in} Mode (Analog)

This is a dip switch that allows the analog V_{in} software register to be overwritten. This switch should be in the *up* position so that the software register is not overwritten. If this switch is in the *down* position, the subsystem will be expecting an analog V_{in} signal.

Software control of the Analog V_{in} Mode is done through register 7 bit 0, which is on the MIF board. If this bit is 0, then the gradients are in a nonanalog V_{in} Mode, as is the case for the Signa Horizon. If this bit is set to 1, the gradient subsystem is in the Analog V_{in} Mode, as is the case for Signa Horizon HiSpeed and Signa Horizon EchoSpeed. This register is controlled for the gradient driver Tests.

This signal is input to the MIF and is analog coming from the GRAM for HiSpeed and EchoSpeed options. For the Signa Horizon base model, this signal is digital, and comes from the GAP.

8-4-4 Full Scale (FS 200)

Full Scale is a dip switch on the front of the MIF module. It should always be in the *up* position. Register 6 bits 0 and 1, which are software controlled, are set to 11. This causes the output scale to be maximum, or Full Scale. For Signa Horizon, the output is ±200A. For systems with a GRAM, HiSpeed and EchoSpeed option, full scale is ±200V for each power module.

8-4-5 Voltage Control (Control V) Mode

The CNTRL dip switch should always be in the *up* position. For Signa Horizon, the software controlled register 7 bit 2 is set to 0. VCNTL on the GRAM is proportional to VMIF.

8-4-6 Proportional Integrator (PI) Controller

The PI controller is part of the control loop. The P, or proportional circuitry, allows the control loop to react quickly to ramps on the waveform. The I, or integrator circuitry, gives the loop the ability to settle on plateaus very quickly to match the input waveform from the PSD. These two factors are programmable, but are set to a constant value. The purpose of this control loop is to regulate the coil current to match the input waveform from the PSD.

9- GRADIENT DRIVER TROUBLESHOOTING TOOLS

Description - This material outlines the troubleshooting tools that are available for various Signa Horizon Lx systems.

9-1- Introduction

The new gradient driver subsystem was analyzed and scrutinized from a Service Methods perspective. The new approach to troubleshooting this complex closed-loop analog circuit is to look for high-probability modes of failure. The results of these tests and tools assure you of finding high-probability failure modes.

9-2- Gradient Driver Troubleshooting Tools

9-2-1 Error Log

Extended error log (proprietary) – gradient driver subsystem only (see the procedure for Extended Error Log).

9-2-2 Interconnects/Block Diagrams

Gradient driver interconnect/block diagram (nonproprietary)

- Signa Horizon
- Signa Horizon HiSpeed
- Signa Horizon EchoSpeed 8645 gradient amplifier cabinet functional block diagram (proprietary)

GRAM functional block diagram (nonproprietary)

9-2-3 Diagnostics

9-2-3-1 Power-up Diagnostics

New gradient driver power-up diagnostics (nonproprietary) for hardware configuration verification and digital communication path. (See the procedure for Gradient Driver Power-up Diagnostics.)

9-2-3-2 TPS Peripheral Diagnostics

New gradient driver tests (proprietary) with ASM GASM Local Voltage Check, static tests, and dynamic (analog) tests all invoked with the touch of one button. Strategically designed to build confidence in high-probability failure modes on hardware being tested at key points in the closed-loop circuit. (See the procedure for Gradient Driver Tests.)

9-2-3-3 Manual Diagnostics

- Manual Gradient Driver Tests: A series of tests (nonproprietary) that use a strategically planned troubleshooting flowchart to isolate high probability failure modes to the FRU. (See the procedure for Manual Gradient Driver Tests).

- Dynamic Settling Time Test (nonproprietary) (See the procedure for Dynamic Settling Time Test).
- Transformer Core Temperature Test (nonproprietary) (See the procedure for Transformer Core Temperature Test).
- Transistor Junction Temperature Test (nonproprietary) (See the procedure for Transistor Junction Temperature Test).
- Output Shelf Temperature Test (nonproprietary) (See the procedure for Output Shelf Temperature Test).
- Dac_DI Voltage Offset Test (nonproprietary) (See the procedure for Dac_DI Voltage Offset Test).
- SHMOD (proprietary) (See the procedure for SHMOD).
- Hardware Status Check (proprietary) (See the procedure for Hardware Status Check).
- Shorted Transistor Shelf Test (nonproprietary) (See the procedure for Shorted Transistor Shelf Test).
- Load Continuity Test (nonproprietary) (See the procedure for Load Continuity Test).

9-2-5 Functional Checks

The 8645 gradient driver checks (nonproprietary) functional checks (See the procedure for 8645 Gradient Driver Checks).

9-2-6 Swapping Components

GRAM Troubleshooting Harness (proprietary) (See the procedure for GRAM Troubleshooting Harness).

9-2-7 Theory of Operation (proprietary): Gradient Driver Subsystem

- Gradient driver system overview: Section 1
- IPG board changes: Section 2.
- GAP board theory: Section 3.
- MIF Theory: Section 4.
- ASM / GASM theory: Section 5.

- Power modules theory: Section 6.
- GRAM theory: Section 7.
- Gradient driver signal overview theory: Section 8.

REVISION HISTORY

REV	DATE	AUTHOR	PRIMARY REASONS FOR CHANGE
0	May 28, 1998	J. Saperstein	Initial conversion from Toolbook to Word.
1	October 13, 1999	K. Keshena	Changed to proprietary header.